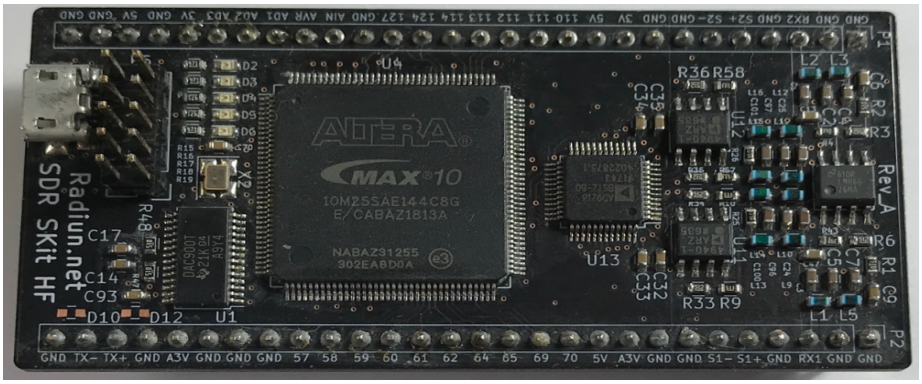
Recombination SDR signal processing blocks

SDR Block HF



User Manual

Radiun

http://radiun.net/

 Model:SBH-1 Revision A

Table of contents

Features

The SDR Block HF is LF to HF band Transceiver based on the SDR technology. SDR is consisted of 20 or more items of signal processing blocks on the FPGA. Connections of these SDR blocks are recombined by software control without FPGA compile and configuration.

To recombine SDR blocks and capture wave data to PC, The SDR Block HF are providing easy access to user USB connection.

By using SDR Block HF own EXCEL macro SDR_ASM, SDR blocks are recombined and capture wave data easily via USB. A documented USB bridge FT232HL SPI allows developers to create new applications.

The SDR Block HF provides SDR experiment features ideally suited to industrial, scientific and educational applications.

High resolution NCO

Generate 5Hz to 32MHz 5Hz step Sin wave. Adjustable Amp, Phase and DC offset independently.

18x17 Matrix BUS Switch

Large 18 x 17 size matrix connection of SDR blocks is build from 17 rows and 18 columns of 12bit parallel BUS.

Variable Decimation filter

4 steps CIC filter is adjustable decimation rate 1 to 32000.

17 select CLK freq.

Each SDR blocks are able to select 17 steps of Clock frequency independently.

4096 word AWG x2ch

12bit x 4096 x 2ch AWG
Clock adjustable 128MHz to 2kHz.

40dB LNA x2ch for RX

LNA is TI OP amp LMH6626.
GBW 1.5GHz, 1nV/√Hz.
Gain 40dB and 20dB buffer amp.

JTAG DIP 2x5 pins

Rewriteable CONFIG data accompanied with updating FPGA revision.

High speed USB

Up to 12Mbps available allows developer create real time signal processing applications on the PC.

Key Features

RX/TX Frequency Range：10kHz～32MHz
RX/TX Bandwidth：32MHz(64Msps)/ch
ADC: 10bit 64Msps x2ch for RX input
ADC: 12bit 1Msps for Audio input
DAC: 10bit 64Msps for TX output
PWM: 11bit 64ksps for Audio output
Sensitivity： −110dBm/10kHz typ. S/N=10dB
TX output: 1Vp-p diff (No Load)
NCO: 64Msps 5Hz resolution x2ch
Digital filter: CIC x2ch Variable Decimation
AGC: Variable 17 speed response
AWG: 12bit x 4096 x 2ch
Wave Capture: 12bit x 1024 x 2ch via USB
Other blocks: Adder, Mixer, Square, Square Root and Constant level.
USB: FTDI FT232HL SPI in MPSSE mode
Power: DC 5V 500mA via USB available
Size: 3.0 x 1.4 inch 2 x 28 pin DIP

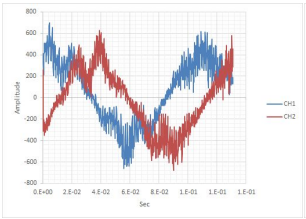
Applications

Amateur Radio Transceiver, Spectrum Analyzer, VNA, AWG, Signal Generator, Ultra Sonic Rader, Logger

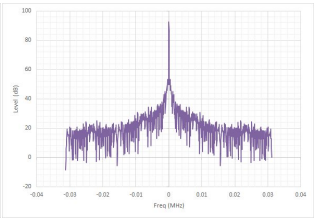
Controller of the SDR Block HF

SDR ASM FREE

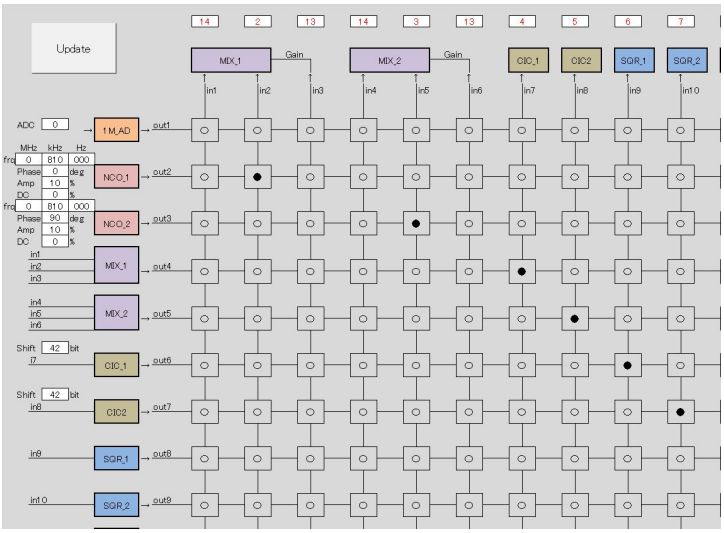
The SDR_ASM on the EXCEL controls recombination of SDR blocks, change parameters and clocks, AWG data transfer and capturing wave data.



Time domain I/Q



FFT

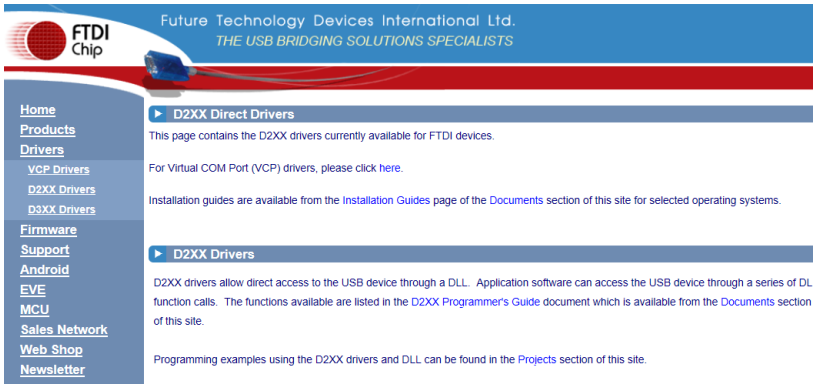


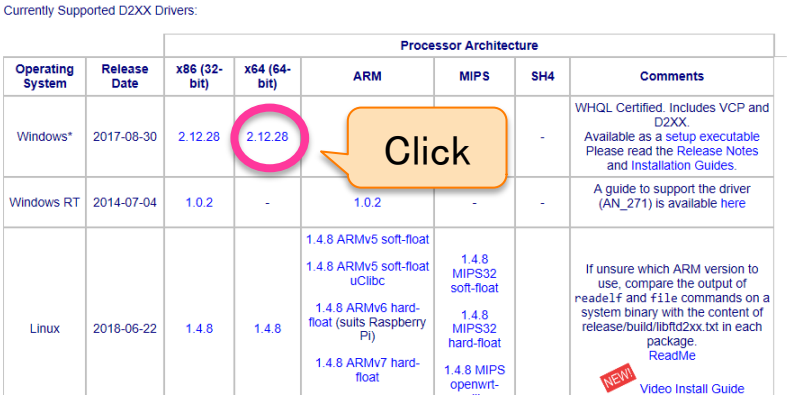
18x17 Matrix BUS Switches

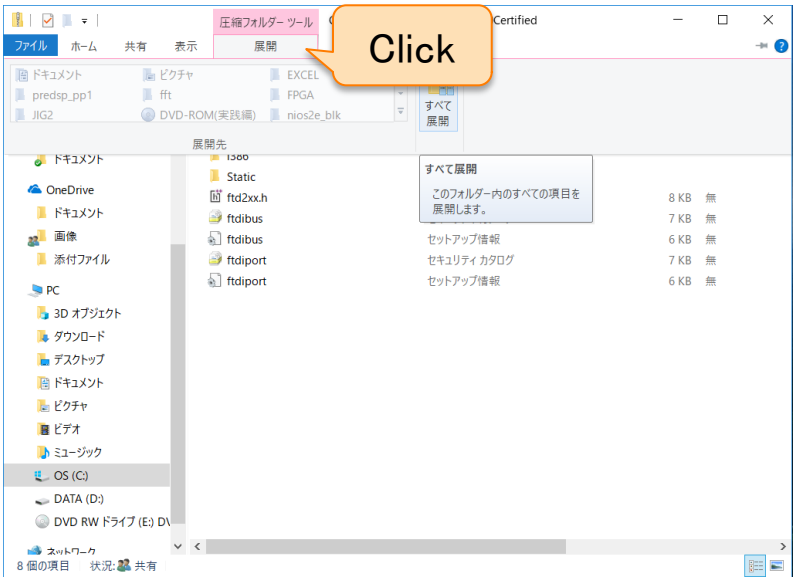
Quick Start

1. Install FTDI Driver (Windows10)

https://www.ftdichip.com/Drivers/D2XX.ftml

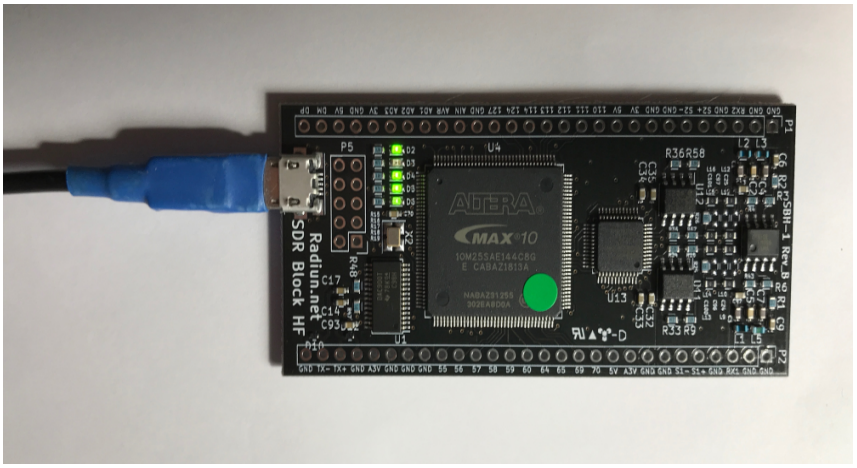




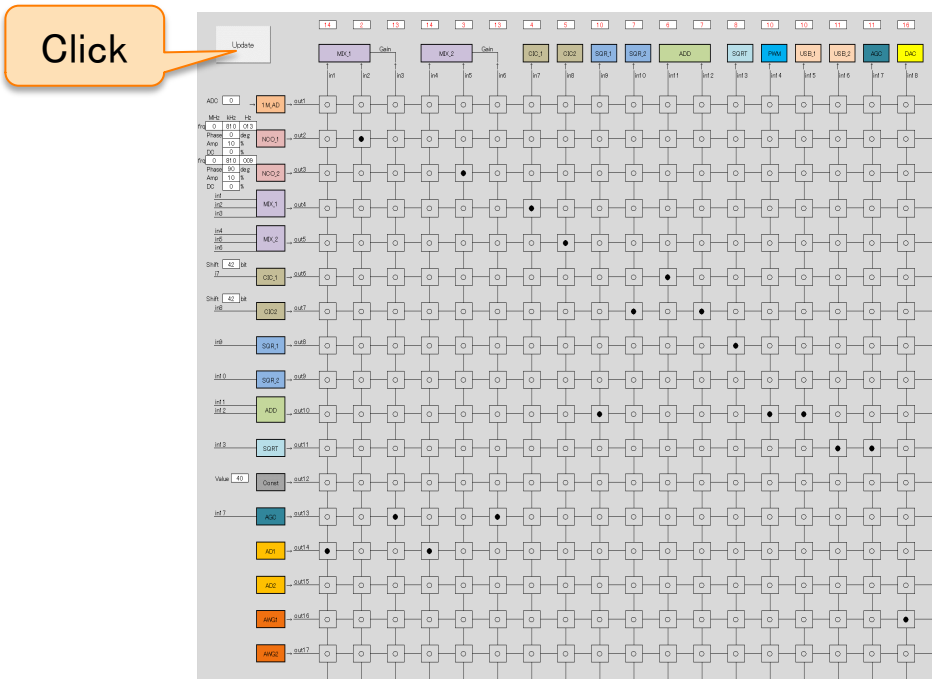


Unzip and locate download file to Desktop or any folder.

2. Connect PC and SBH-1 board via USB



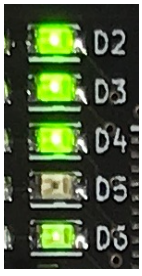
Connect USB cable to PC. Check LED light on like picture above.



Launch an Excel sheet “SDR ASM” and open Worksheet “Blocks”.
Then click “Update” button to send any data to SBH-1 board.

After
Power ON

Success
Connect USB



Check LED after click “Update” button.

D2 : Divided master clock 1sec interval

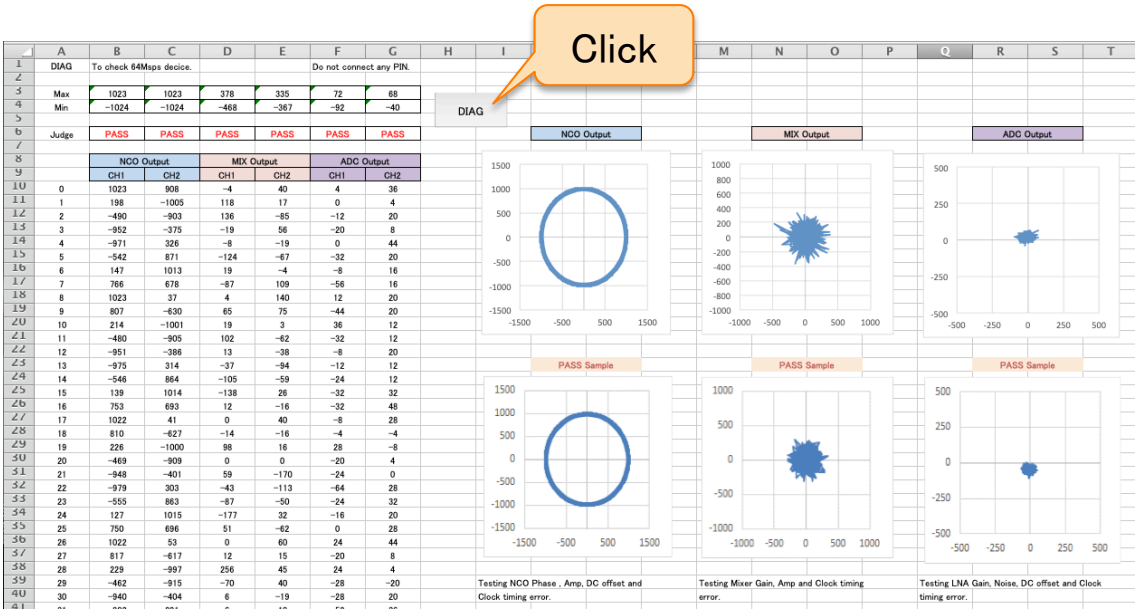
D3 : NCO Reset. 0:Reset 1:Run

D4 : SPI CE 0:Enable 1:Disable

D5 : SPI CLK 0:No Clock 1:Clocking

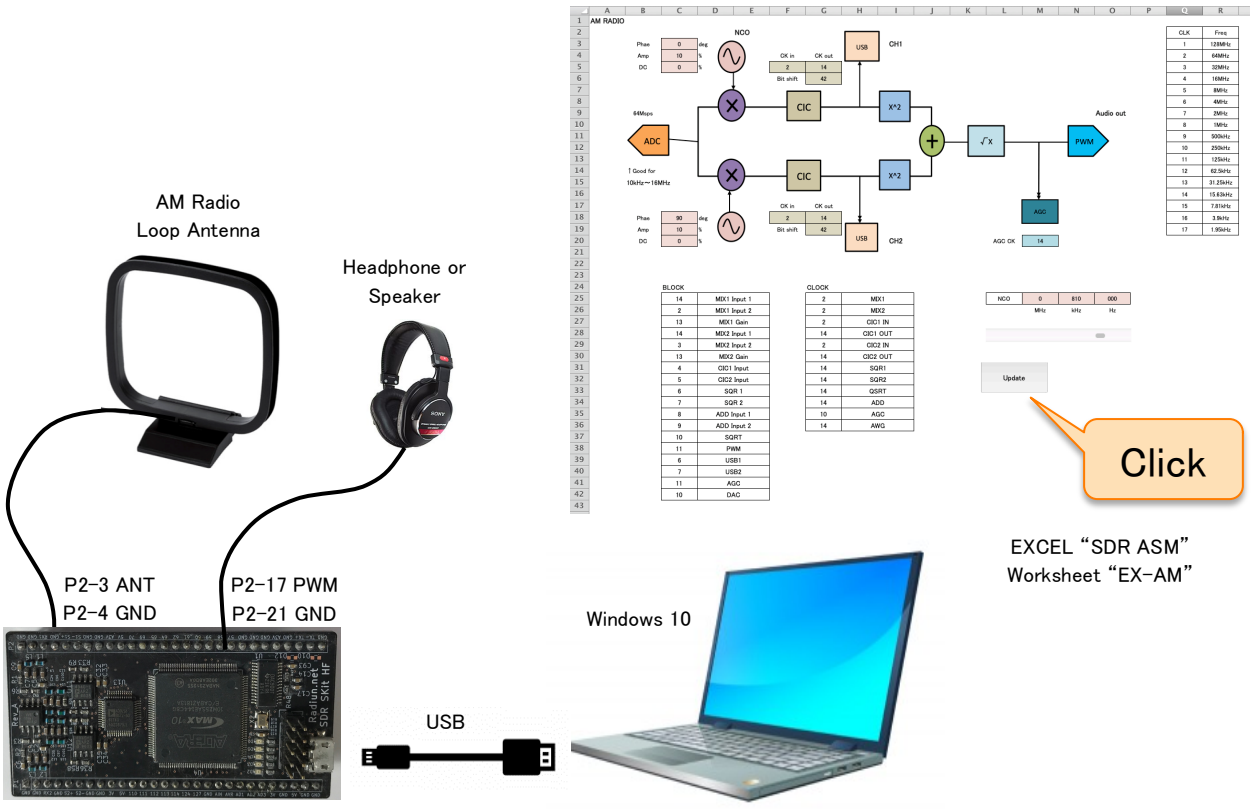
D6 : FTDI 12MHz CLK

3. Execute Diagnostic (DIAG)



Disconnect all of the SBH-1 pins except USB. Launch an Excel sheet “SDR ASM” and open Worksheet “DIAG”. Then click “DIAG” button to diagnose the SBH-1 board itself automatically.

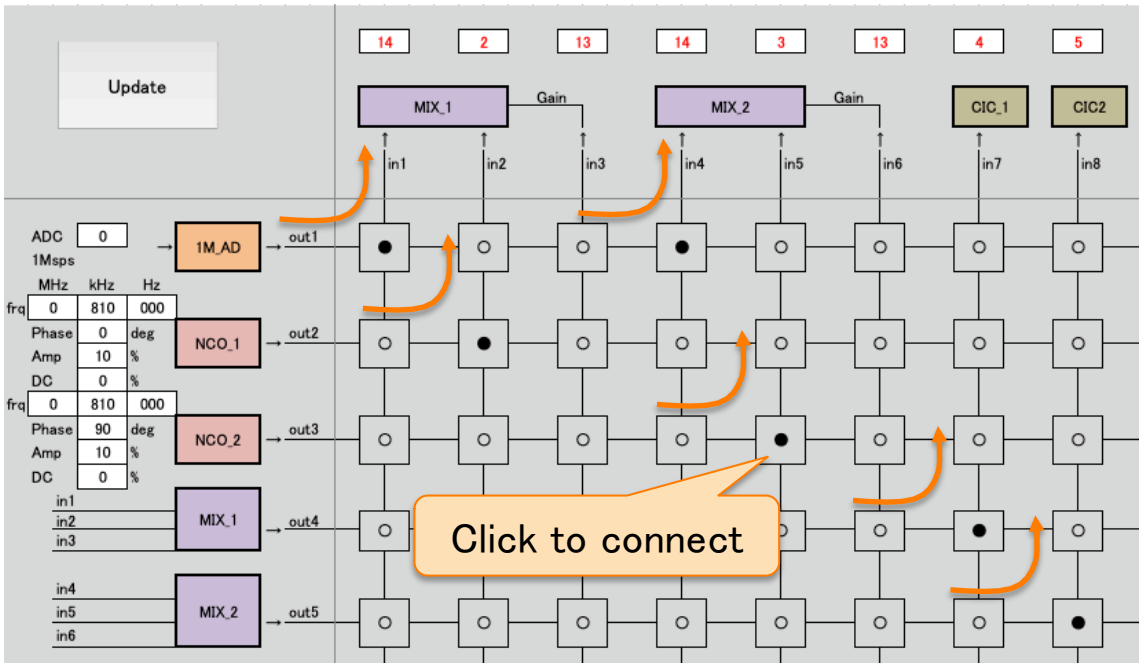
4. Build AM RADIO



Connect Loop antenna and headphone to SBH-1. Launch an Excel sheet “SDR ASM” and open Worksheet “EX_AM”. Click “Update” button to build AM RADIO circuit on the FPGA.

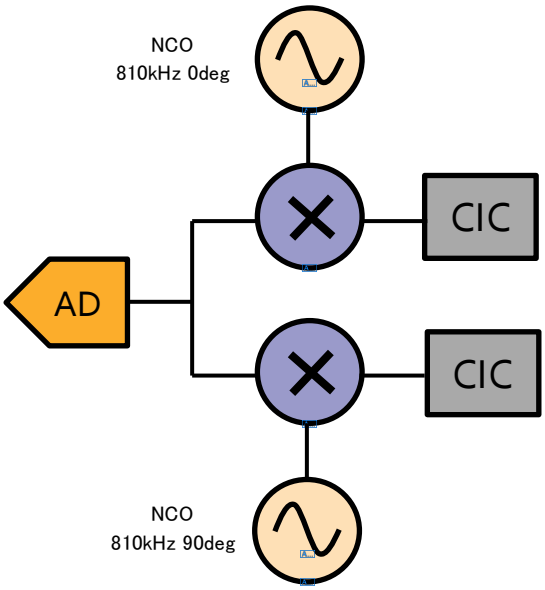
Define Blocks

1. Define Block Diagram

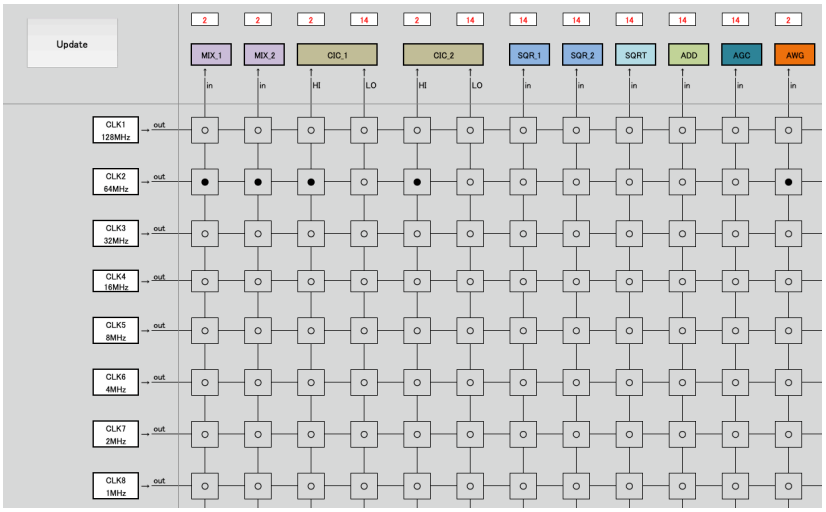


A FPGA on the SBH-1 consists of 20 items of signal processing brocks and 18x16 matrix BUS switch. BUS switch is software controlled via USB like above. Click to connect BUS on the cross point on Worksheet “Blocks”.

The above example is shown as follows.



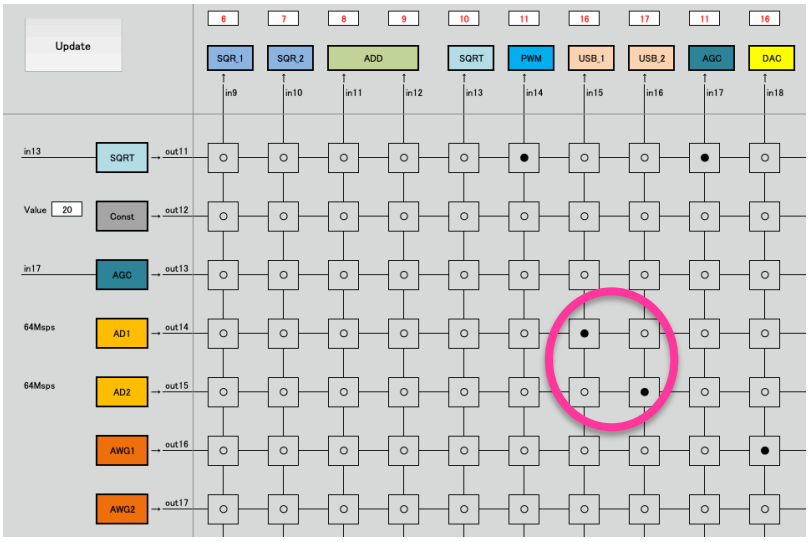
2. Define Clock Frequency



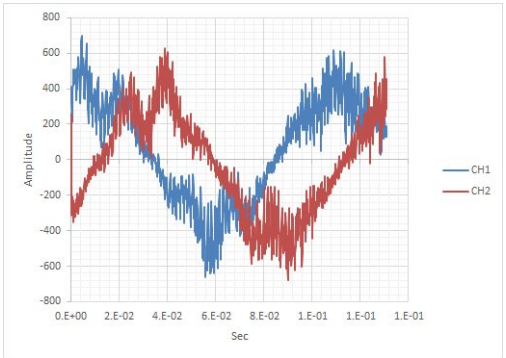
SDR signal processing blocks are able to select 17 frequency clocks. 2kHz to 128MHz. ADC and NCO are fixed 64MHz. It becomes possible to change CIC filter cutoff, adjustable AGC response and adjustable AWG speed.

Recommend Clock frequency is 64MHz or lower. Be careful, as the operation is not guaranteed 128MHz clocks.

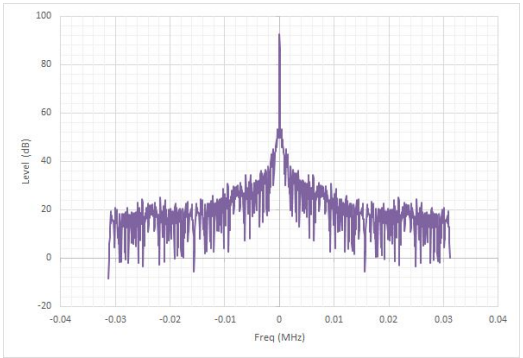
3. Define Test points



Test points (USB 1/2) can be placed in the circuit where you want to place. Results are displayed time domain like a Oscilloscope or frequency domain like a Spectrum analyzer on the EXCEL sheet.



Time domain I/Q

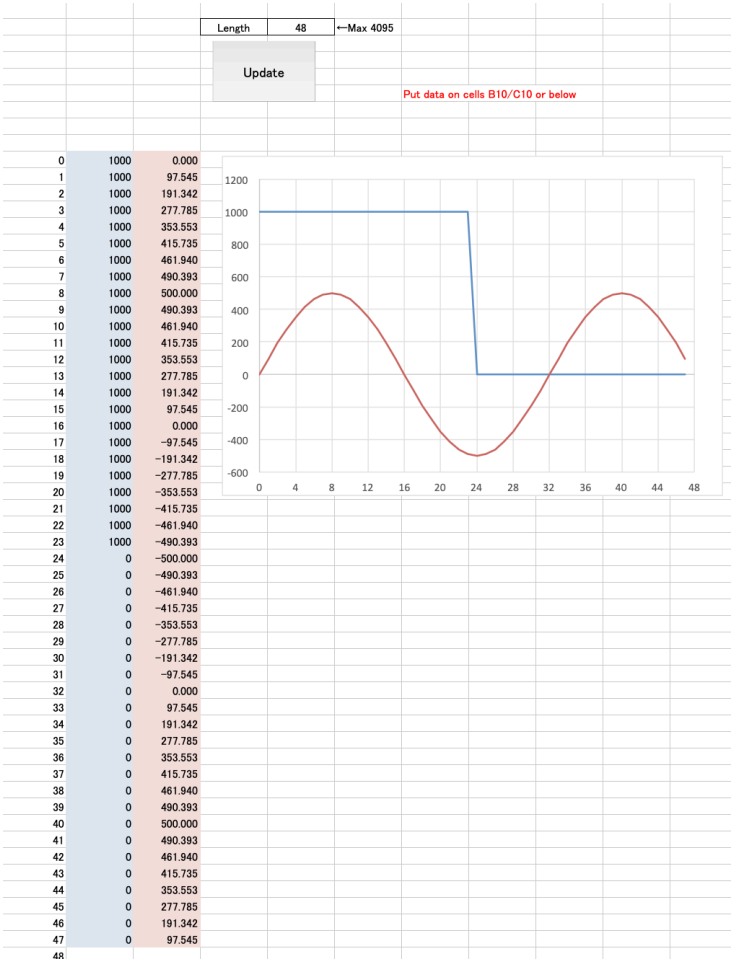


FFT

AWG

Arbitrary Waveform Generator

AWG1 and AWG2 blocks are the arbitrary waveform generator (AWG). Waveform editing and update wave data to RAM can be done with Excel “”SDR ASM” worksheet “AWG”. AWG clock is selectable 2kHz to 64MHz.



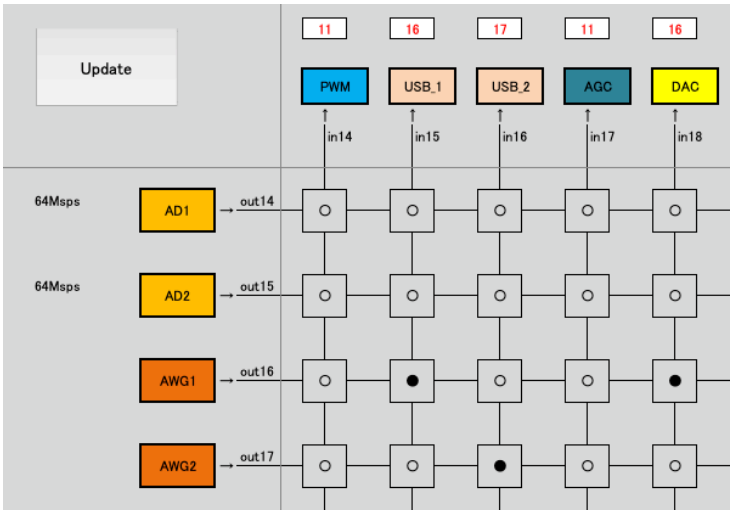
This is worksheet “AWG”.

Available data is signed 12bit −2047 to 2047.

Data length up to 4095 words each.

Push “Update” to update wave data to RAM.

AWG continue generate wave repeat with the specified Data length.

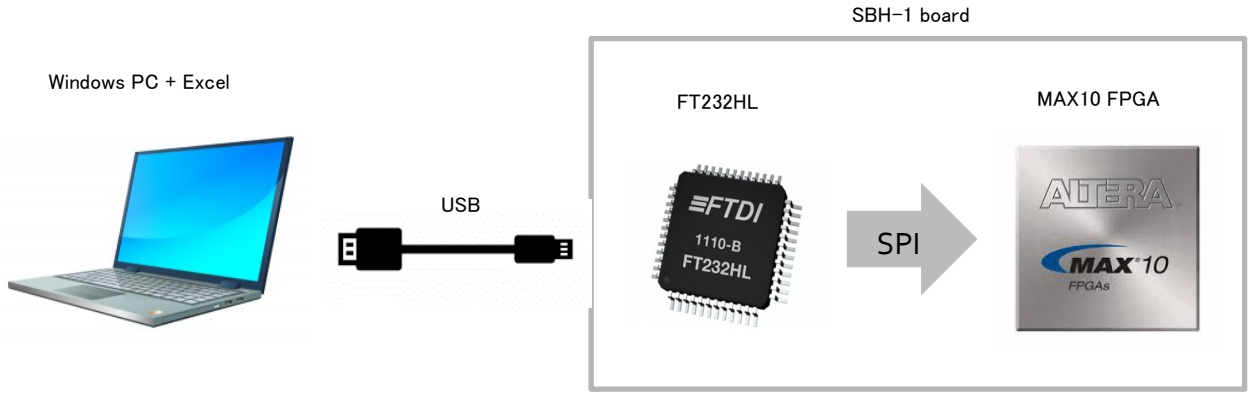


This is worksheet “Blocks”.

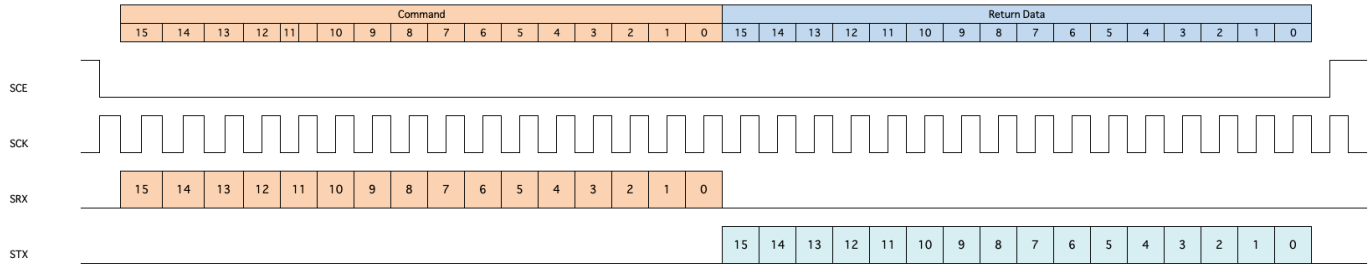
Here is an example for using the AWG1 and AWG2.

Waveform data of the AWG is output to the USB1, USB2 and DAC also.

SPI command



1. SPI Timing Chart



2. SPI Command List

		Command																Return Data															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Func				Parameter												16bit data																
0	Capture Reset	0	0	0	0	Mode		ADC 5bit						RAM CLK				Not use															
1	Read RAM	0	0	0	1	CH	RAM Address 11bit											Write ADRS			Return RAM Data 12bit												
2	NCO frequency	0	0	1	0	CH	Range 3bit		Freq 8bit									Not use															
3	Constant value	0	0	1	1	Const value 12bit												Not use															
4	Blocks define	0	1	0	0		X 5bit					Y 5bit						Not use															
5	Clock define	0	1	0	1		X 5bit					Y 5bit						Not use															
6	NCO Phase	0	1	1	0	CH	Signed Phase 11bit											Not use															
7	NCO Amp/DC	0	1	1	1	CH	DC	Signed Amp/DC 10bit										Not use															
8	CIC Bit shift	1	0	0	0	CIC1 6bit						CIC2 6bit						Not use															
9	AWG1 data update	1	0	0	1	AWG1 write data 12bit												Read ADRS			Not use												
10	AWG2 data update	1	0	1	0	AWG2 write data 12bit												Read ADRS			Not use												
11	AWG Size	1	0	1	1	AWG Data Size 12bit												Not use															

0	Select ADC, Select Capture Clock, Reset RAM address
1	Select RAM CH, Read RAM data in FPGA to PC
2	Select NCO CH, Set Frequency
3	Set Constant value signed 12bit -2047～2047
4	Define Blocks（X:Input BUS line、Y:Output Bus line）
5	Define Clock(X:Input BUS line、Y:Output Bus line)
6	Set NCO Phase 0～804 (0～180deg)
7	Set NCO Amplitude or DC offset 0～1023 (0～100%)
8	Specify the BIT position to extract the signal
9	Write AWG1 data to RAM in the FPGA with increment address.
10	Write AWG2 data to RAM in the FPGA with increment address.
11	Set AWG data length and Reset RAM address.

3. Detail of the SPI Command

0. Capture Reset

Command																Return Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Func				Parameter												16bit data																

0	0	0	0	Mode	ADC 5bit	RAM CLK	Not use

Before capturing the waveform in FPGA to RAM, execute this command and Reset both address to CH1 and CH2.

At the same time, set the following parameters related to waveform capture.

Mode (Capture mode)				
		0	Single	Stop capturing 2048 words in RAM
		1	Stream	Continually capture waveform repeatedly in RAM
	0		PWM OFF	PWM output serves as a noise source, the PWM signal is stopped.
	1		PWM ON	Release PWM stop.

ADC (1Msps ADC)						
0	0	0	0	0	Analog IN	Select the input pin of the MAX10 ADC to Analog IN(AIN).
0	0	0	0	1	ADC1	Select the input pin of the MAX10 ADC to Analog IN(AD1).
0	0	0	1	0	ADC2	Select the input pin of the MAX10 ADC to Analog IN(AD2).
0	0	0	1	1	ADC3	Select the input pin of the MAX10 ADC to Analog IN(AD3).

RAM CLK				
0	0	0	0	Not Available
0	0	0	1	128MHz
0	0	1	0	64MHz
0	0	1	1	32MHz
0	1	0	0	16MHz
0	1	1	1	8MHz
0	1	1	0	4MHz
0	1	0	1	2MHz
1	0	0	0	1MHz
1	0	1	1	500kHz
1	0	1	0	250kHz
1	0	0	1	125kHz
1	0	0	0	62.5kHz
1	1	1	1	31.25kHz
1	1	1	0	15.63kHz
1	1	0	1	7.81kHz
1	1	1	0	3.9kHz
1	0	1	1	1.95kHz

Set the clock for loading the waveform into the RAM in FPGA.

1. Read RAM

Command																Return Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Func				Parameter												16bit data																

0	0	0	1	CH	RAM Address 11bit			Write ADRS	Return RAM Data 12bit

Specify the CH and address of the RAM to be read and obtain its contents as Return.

CH	
0	CH1
1	CH2

Select CH of RAM to be read.

RAM Address 11bit										
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1

Return the RAM contents of the address specified here as Return Data.

Address=0

Address=1

Address=2046

Address=2047

Write ADRS			
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0

Return the upper 4 bits of the address currently written to the RAM. This is for Stream captureing mode.

Writing RAM address 128 or upper.

Writing RAM address 256 or upper.

Writing RAM address 512 or upper.

Writing RAM address 1024 or upper.

Return RAM Data 12bit											
0	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	0
1	0	0	0	0	0	0	0	0	0	0	0

It returns the data of the specified RAM address in 2's complement.

Data=2047

Data=1

Data0

Data=−1

Data=−2047

2. NCO Frequency

Command																Return Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Func				Parameter												16bit data																

0	0	1	0	CH	Range 3bit	Freq 8bit	Not use

Set the NCO frequency.

CH	
0	CH1
1	CH2

Set channel of the NCO .

Range (Freq range)			
0	0	0	LOW
0	0	1	MID
0	1	0	HI
1	1	0	NCO Reset ON
1	1	1	NCO Reset OFF

Set the freq data of 24 bits by dividing it into 8 bit by 3 times.

Lower 8 bit data F1= Round(Fo and 0xFF) Fo = Round(F * 0.205887) F(Hz)

Middle 8 bit data F2= Round(Fo and 0xFF00) / 0x100

Upper 8 bit data F3= Round(Fo and 0xFF0000) / 0x10000

After set NCO, this reset is always executed to synchronize the phase CH1 and CH2.

Release of NCO reset.

Freq 8bit								Frequncy data F1, F2 or F3
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

3. Constant Value

Command																Return Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Func				Parameter												16bit data																

0	0	1	1	Const value 12bit	Not use

Set the constant value. Sometimes it is taken as DC offset.

Const value 12bit												
0	1	1	1	1	1	1	1	1	1	1	1	Data=2047
0	0	0	0	0	0	0	0	0	0	0	1	Data=1
0	0	0	0	0	0	0	0	0	0	0	0	Data0
1	1	1	1	1	1	1	1	1	1	1	0	Data=-1
1	0	0	0	0	0	0	0	0	0	0	0	Data=-2047

4. Blocks Define, 5. Clock Define

Command																Return Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Func				Parameter												16bit data																

0	1	0	0		X 5bit	Y 5bit	Not use
0	1	0	1		X 5bit	Y 5bit	Not use

Define Blocks or Define Clock.

X 5bit					Y 5bit					
0	0	0	0	0	0	0	0	0	0	X = 0 Y = 0
0	0	0	0	1	0	0	0	0	1	X = 1 Y = 1
1	1	1	1	0	1	1	1	1	0	X = 30 Y = 30
1	1	1	1	1	1	1	1	1	1	X = 31 Y = 31

6. NCO Phase, 7. NCO Amplitude or DC Offset

Command																Return Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Func				Parameter												16bit data																

0	1	1	0	CH	Unsigned Phase 11bit		Not use
0	1	1	1	CH	DC	Signed Amp/DC 10bit	Not use

Set the NCO phase, amplitude and DC offset.

CH	
0	CH1
1	CH2

Set the NCO channel.

Signed Phase 11bit										
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1
0	1	1	0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0	1	0	0

Set the NCO phase

0	Phase = 0.0 deg
1	Phase = 0.2 deg
803	Phase = 179.8 deg
804	Phase = 180.0 deg

Ralation betoween freq and phase resolution.

MHz	Phase	
1	5.6	
5	28.1	
10	56.3	
16	90.0	←Limit of I/Q
32	180.0	←Limit of Generate

DC	
0	Amplitude
1	DC offset

Select Amplitude or DC offset

Signed Amp/DC 10bit									
0	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	0
1	0	0	0	0	0	0	0	0	0

Set the NCO Amplitude or DC offset.

1023

1

0

−1

−1023

8. CIC Bit Shift

Command																Return Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Func				Parameter												16bit data																

1	0	0	0	CIC1 6bit	CIC2 6bit	Not use

Specify the position to extract 12 bits from the internal register of the CIC.

CIC1 6bit						CIC2 6bit						
0	0	0	0	0	0	0	0	0	0	0	0	CIC1 = 0 CIC2 = 0
0	0	0	0	0	1	0	0	0	0	0	1	CIC1 = 1 CIC2 = 1
1	1	1	0	1	1	1	1	1	0	1	1	CIC1 = 59 CIC2 = 59
1	1	1	1	0	0	1	1	1	1	0	0	CIC1 = 60 CIC2 = 60

↑ When CLK IN = 64MHz CLK IN = 2kHz, the gain is maximum 60dB

9-10. AWG1/2 Data Update, 11 AWG Size

Command																Return Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Func				Parameter												16bit data																

1	0	0	1	AWG1 write data 12bit	Read ADRS	Not use
1	0	1	0	AWG2 write data 12bit	Read ADRS	Not use
1	0	1	1	AWG Data Size 12bit	Not use	

Transfer AWG data to RAM in the FPGA.

AWG1/2 write data 12bit												
0	1	1	1	1	1	1	1	1	1	1	1	Data=2047
0	0	0	0	0	0	0	0	0	0	0	1	Data=1
0	0	0	0	0	0	0	0	0	0	0	0	Data0
1	1	1	1	1	1	1	1	1	1	1	0	Data=-1
1	0	0	0	0	0	0	0	0	0	0	0	Data=-2047

Data is written to RAM of AWG 1/2, and write address is counted up

Read ADRS				
0	0	0	1	Reading RAM address 128 or upper.
0	0	1	0	Reading RAM address 256 or upper.
0	1	0	0	Reading RAM address 512 or upper.
1	0	0	0	Reading RAM address 1024 or upper.

Returns the upper 4 bits of the address currently being read by the RAM. This is for Stream transmit mode.

AWG Data Size 12bit												
0	0	0	0	0	0	0	0	0	0	0	1	Size = 1
0	0	0	0	0	0	0	0	0	0	1	0	Size = 2
1	1	1	1	1	1	1	1	1	1	1	0	Size = 4094
1	1	1	1	1	1	1	1	1	1	1	1	Size = 4095

Set the data length of AWG after writing data, write address is reset

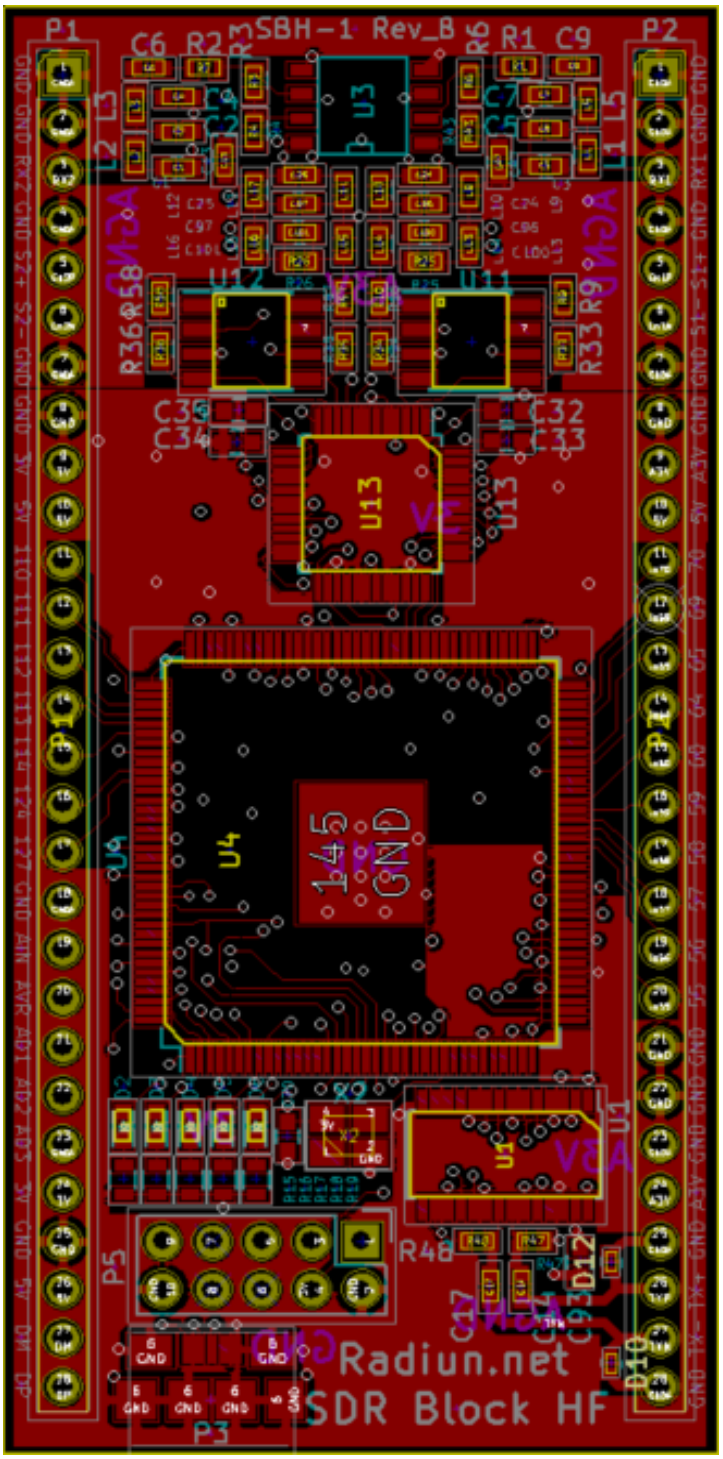
Sample Program (VBA)

This sample program is to read the waveform from the RAM in the FPGA and list the numerical value on the EXCEL sheet when Button is pushed.

```
Sub Oscillo_Click()

    Dim clk As Long

    ' Read Setting CLK and PWM ON/OFF
    clk = Cells(3, 5)
    pwmsw = Cells(12, 10)

    ' Open SPI BUS
    cmd = OpenSPI(0)

    ' RAM addres reset
    'ret = rxSPI(512 + clk + 1024 * pwmsw, 0)   ' Continue mode
    ret = rxSPI(clk + 1024 * pwmsw, 0)          ' Single mdoe

    ' Start Capture
    ret = rxSPI(4096, 0)

    ' Read RAM CH1
    ch = 0
    For n = 0 To 1023
        ret = rxSPI(ch * 2048 + 4096 + n, 0)
        dat = (ret And 4095)                    ' ADC data
        adrs = (ret And 61440)                  ' RAM current address
        If dat > 2047 Then Cells(n + 10, 3) = dat - 4096
        If dat < 2047 Then Cells(n + 10, 3) = dat
    Next

    ' Read RAM CH2
    ch = 1
    ret = rxSPI(ch * 2048 + 4096 + n, 0)
    For n = 0 To 1023
        ret = rxSPI(ch * 2048 + 4096 + n, 0)
        dat = (ret And 4095)                    ' ADC data
        adrs = (ret And 61440)                  ' RAM current address
        If dat > 2047 Then Cells(n + 10, 4) = dat - 4096
        If dat < 2047 Then Cells(n + 10, 4) = dat
    Next

    ' PWM ON
    ret = rxSPI(0, 0)

    ' Close SPI BUS
    CloseSPI

End Sub
```

PIN Layout

P1-01	GNDA
P1-02	GNDA
P1-03	RX2 IN
P1-04	GNDA
P1-05	CH2P NU
P1-06	CH2N NU
P1-07	GNDA
P1-08	GND
P1-09	3V OUT
P1-10	5V IN
P1-11	IO110 NU
P1-12	IO111 NU
P1-13	IO112 NU
P1-14	IO113 NU
P1-15	IO114 NU
P1-16	IO124 NU
P1-17	IO127 NU
P1-18	GNDA
P1-19	ANAIN1
P1-20	VREF
P1-21	ADCIN1
P1-22	ADCIN2
P1-23	GNDA
P1-24	3V OUT
P1-25	GND
P1-26	5V IN
P1-27	USB DM
P1-28	USB DP



JTAG-1	TCK	JTAG-2	GND
JTAG-3	TDO	JTAG-3	3V
JTAG-5	TMS	JTAG-4	NC
JTAG-7	NC	JTAG-5	NC
JTAG-9	TDI	JTAG-10	GND

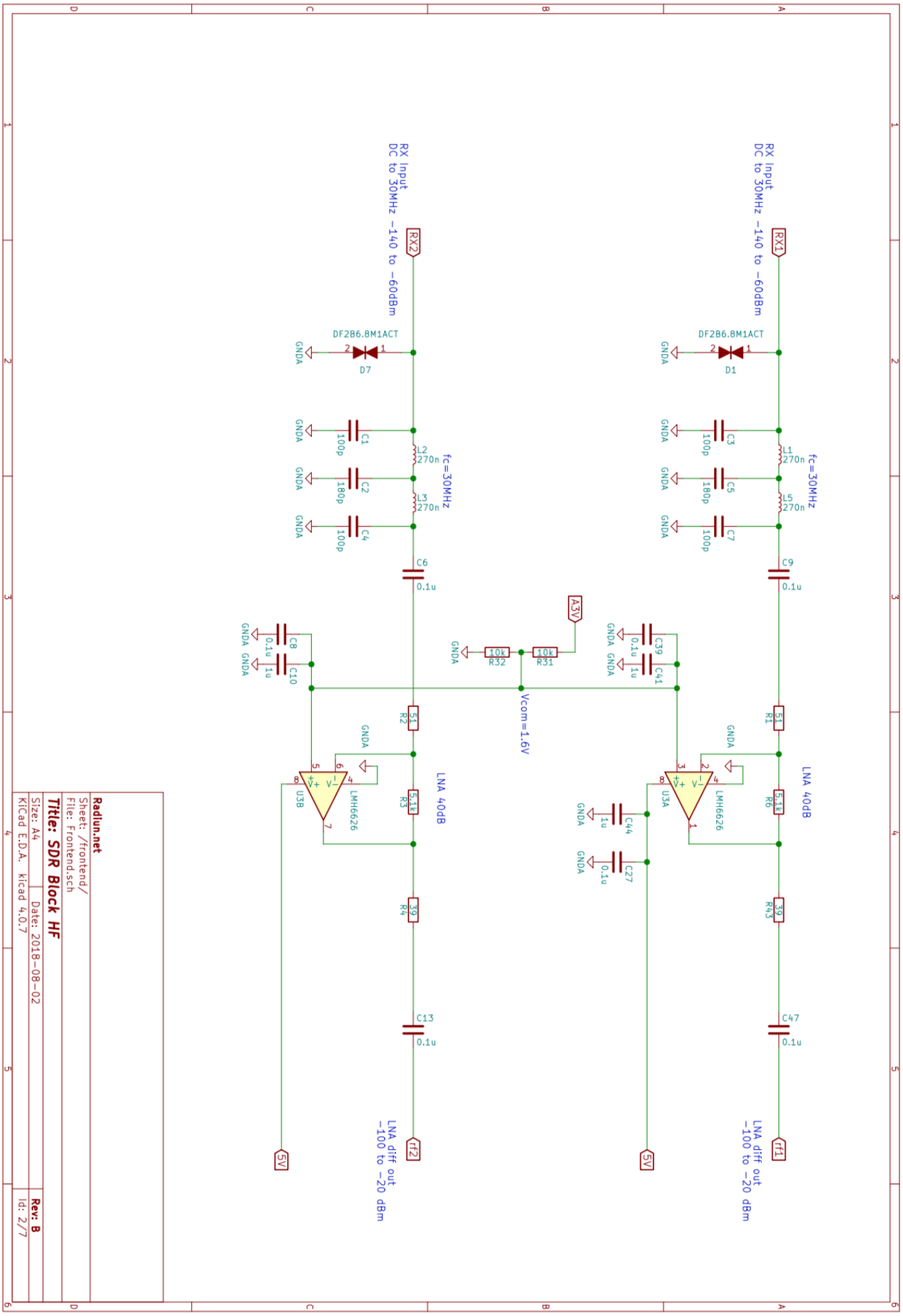
P2-01	GNDA
P2-02	GNDA
P2-03	RX1 IN
P2-04	GNDA
P2-05	CH1P NU
P2-06	CH1N NU
P2-07	GNDA
P2-08	GND
P2-09	3V OUT
P2-10	5V IN
P2-11	IO70 NU
P2-12	IO69 NU
P2-13	IO65 NU
P2-14	IO64 NU
P2-15	IO60 NU
P2-16	IO59 NU
P2-17	IO58 PWM
P2-18	IO57 NU
P2-19	IO56 NU
P2-20	IO55 NU
P2-21	GND
P2-22	GND
P2-23	GNDA
P2-24	3V OUT
P2-25	GND
P2-26	TXP OUT
P2-27	TXN OUT
P2-28	GNDA

NU means Not Use pin but wired on the board. When you want to use it, you can use it by definition or added parts.

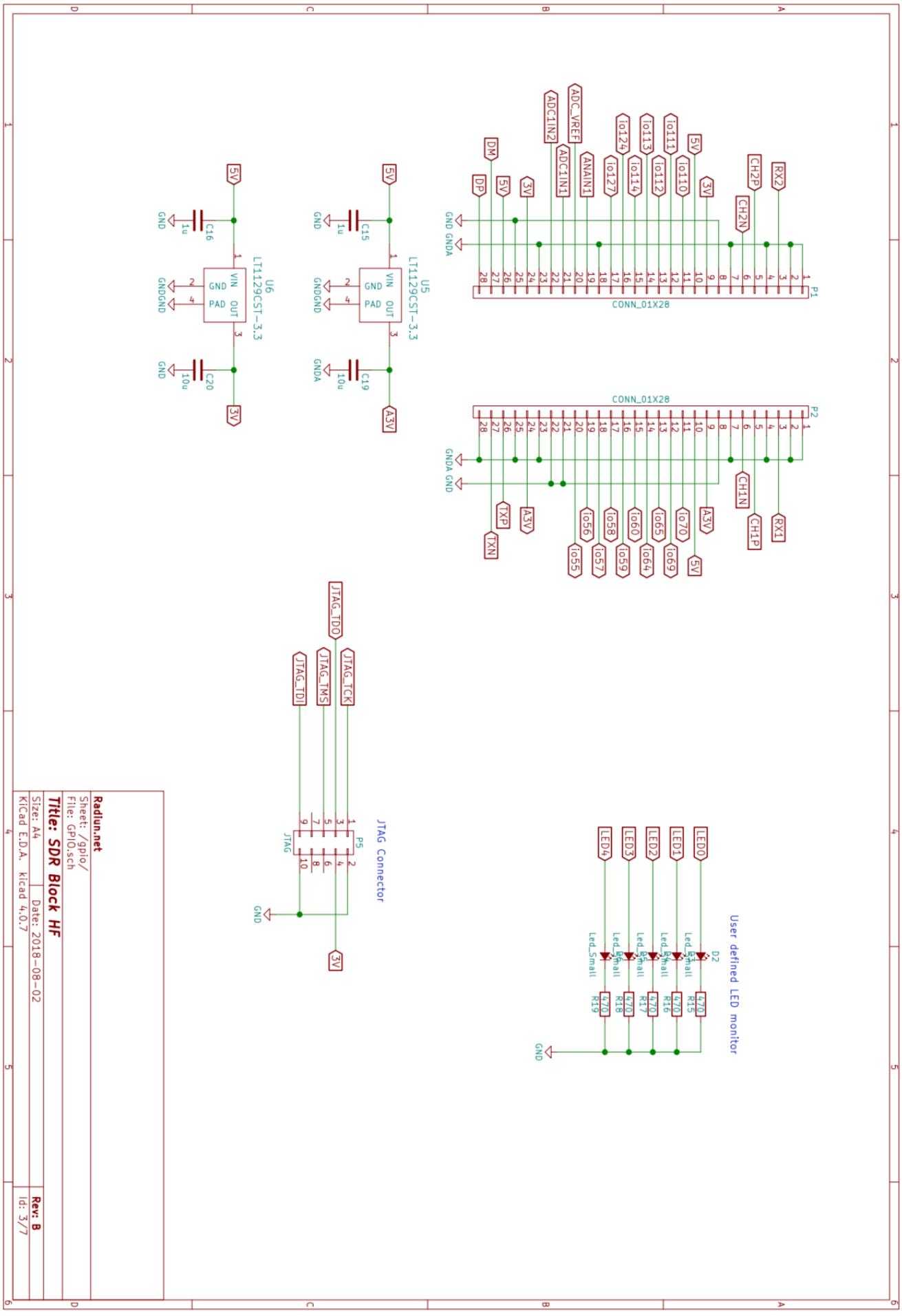
CH1P/N and CH2P/N are differential 64Msps ADC input to pass the 40dB LNA.

Schematics

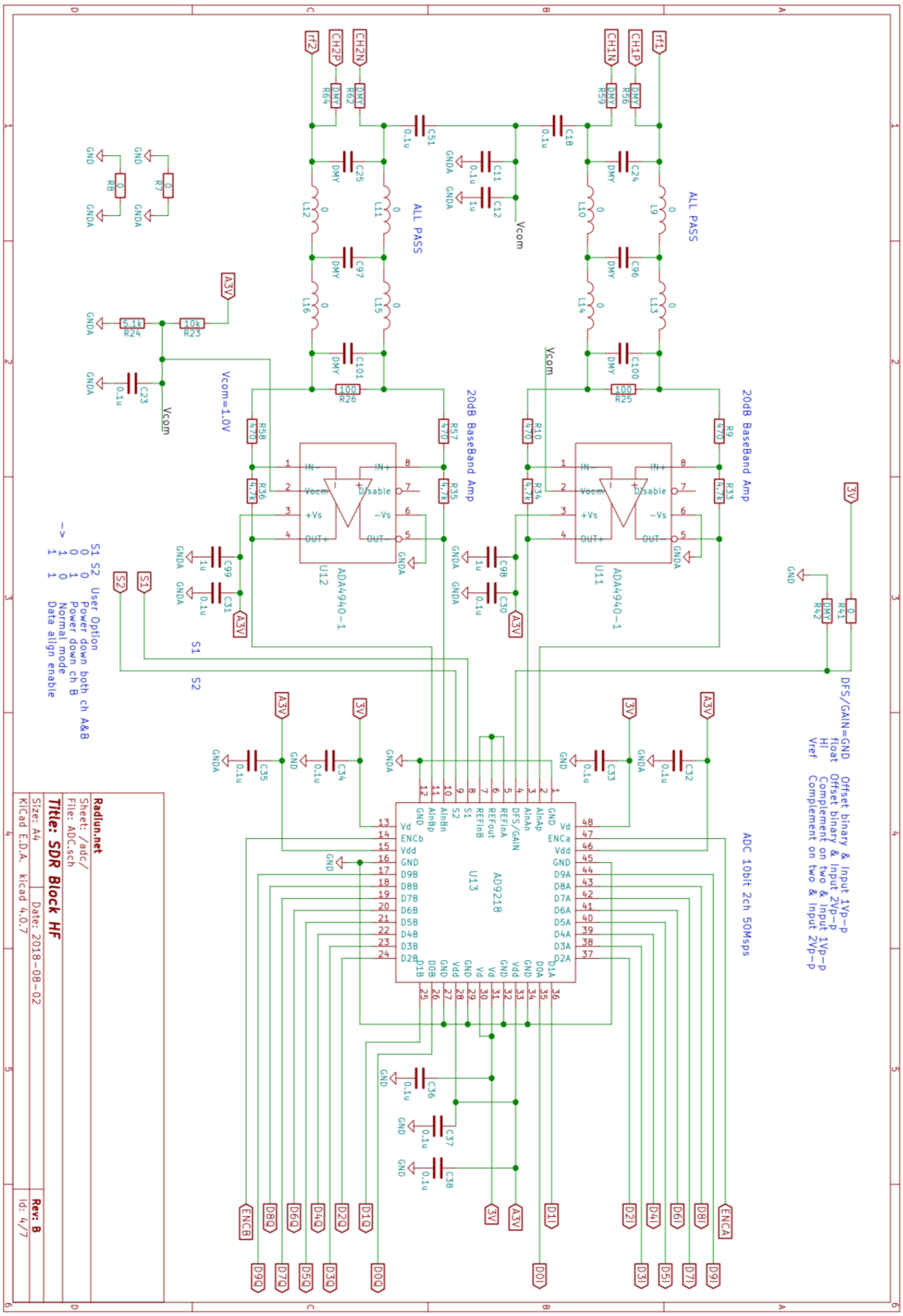
RX Frontend



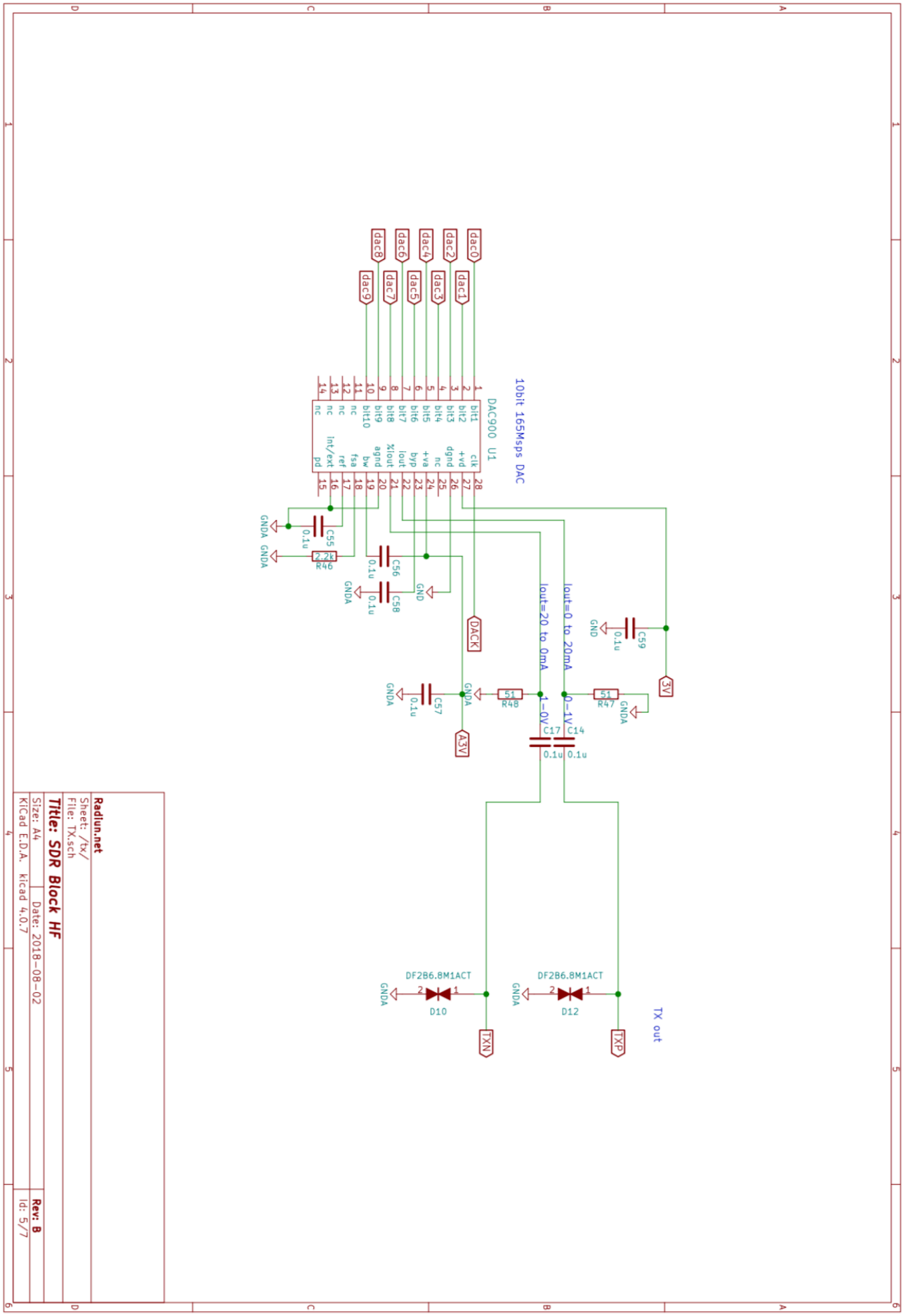
GPIO, JTAG, LDO, LED



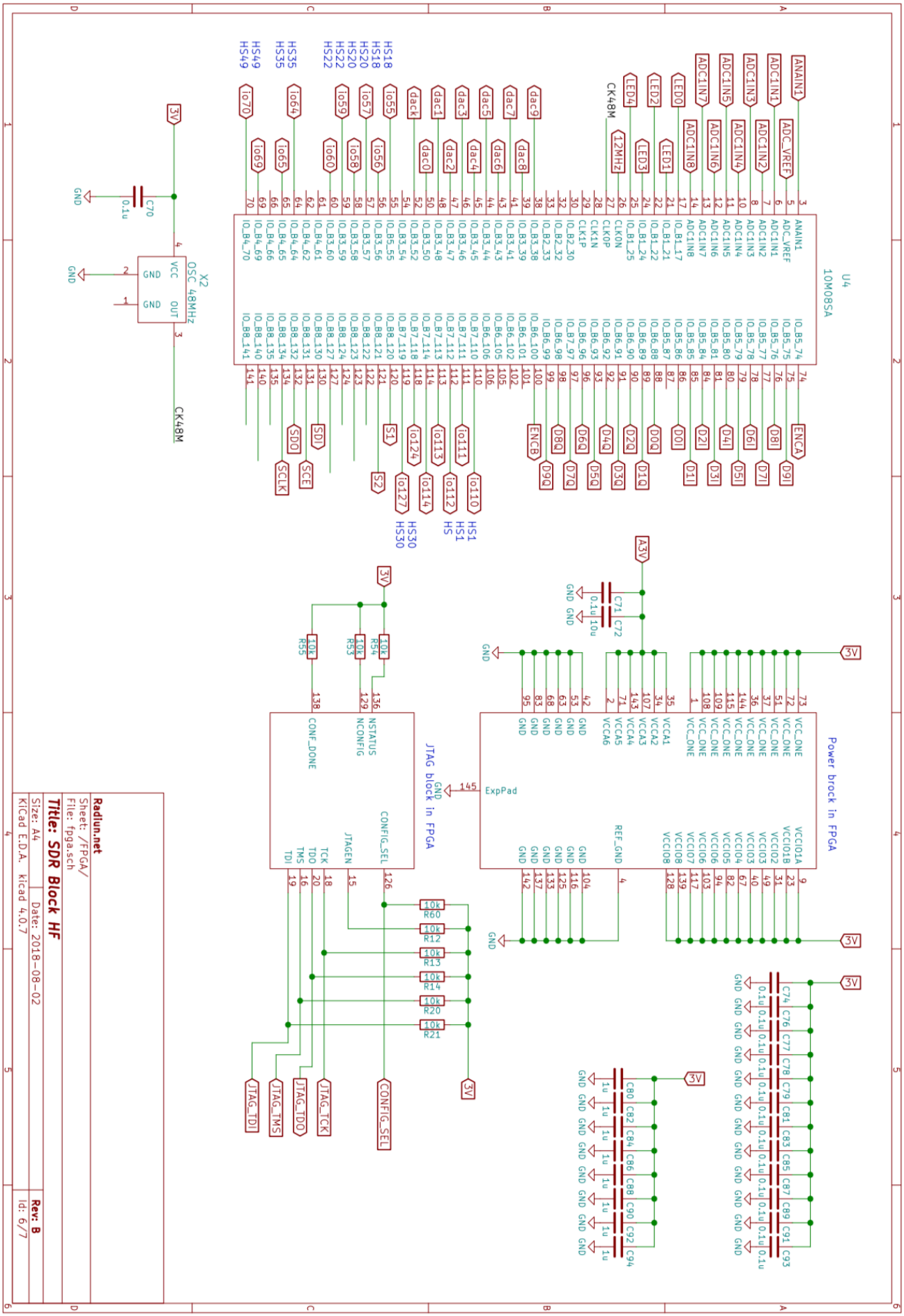
20dB Amp, 64Msps ADC



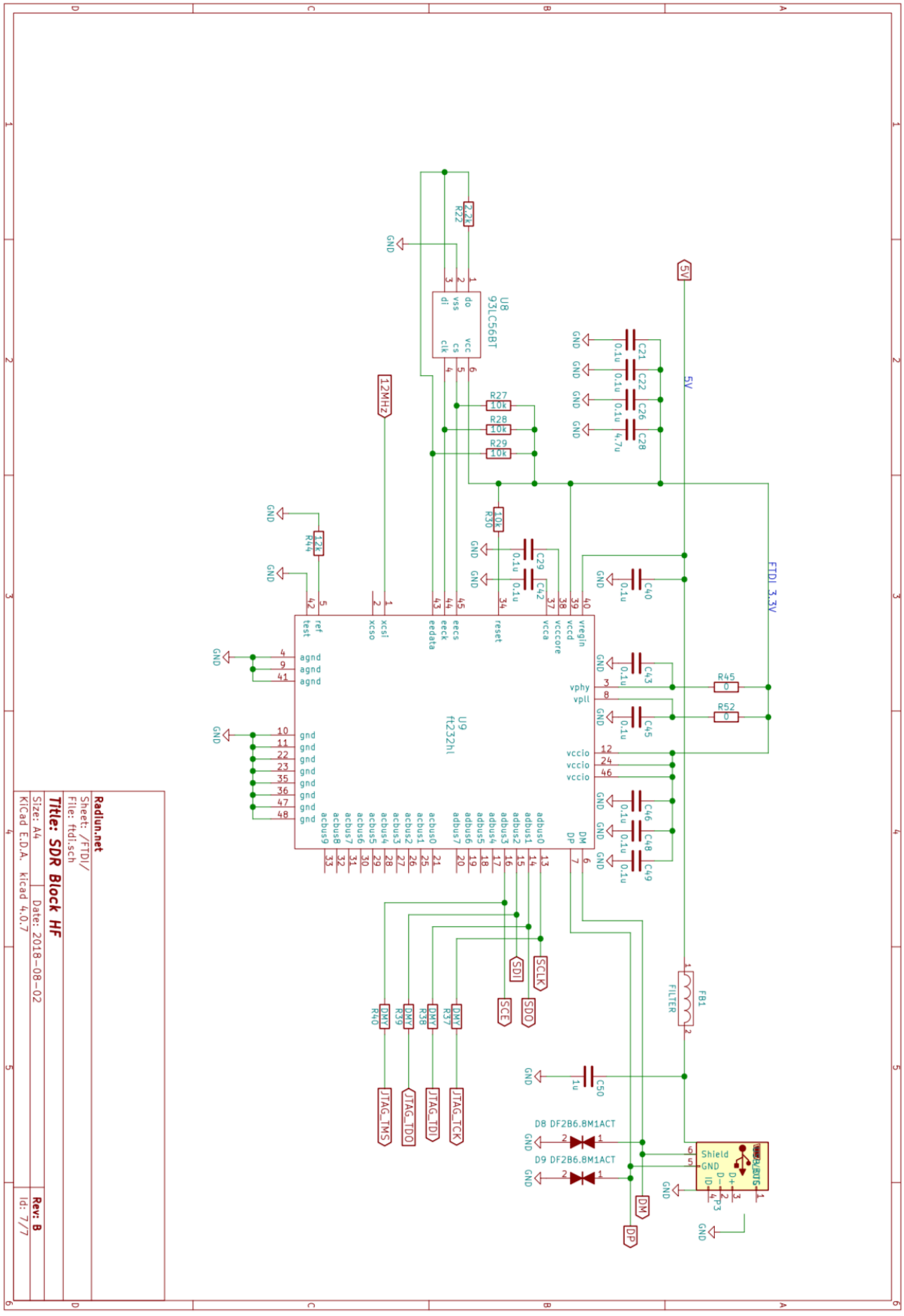
64Msps DAC, TX output



FPGA MAX10, TCXO



USB FTDI


U8
93LC56BT
U9
ft232hl
12MHZ
5V
FTDI 3.3V
SDI
SCLK
SCE
SDO
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK
DM
DP
D8 DF2B6.8M1ACT
D9 DF2B6.8M1ACT
FILTER
FB1
Shield
GND
Radiun.net
Sheet: /FTDI/
File: ftdi.sch
Title: SDR Block HF
Size: A4
Date: 2018-08-02
KiCad E.D.A. kicad 4.0.7
Rev: B
Id: 7/7

Specifications

	Min	Typ	Max	Remarks
Frequency Range	10kHz		32MHz	Nyquist Limit = fsmp/2
	10kHz		16MHz	I/Q Limit = 90deg
Resolution		5Hz		
RX ADC x2ch		10bit 64Msps		AD9218-80Msps
AF ADC x1ch		12bit 1Msps		MAX10 ADC
TX DAC x1ch		10bit 64Msps		DAC900 165Msps
TX Output		1Vp-p		Differential, No Load
RX Gain		60dB		Total
		40dB		LNA LMH6626 x2ch
		20dB		Defferential OP amp ADA4940 x2ch
Noise Floor		-160dBm/Hz		RX input 1MHz
PWM Output		1Vp-p		Differential, No Load
		11bit 62.5ksps		
Power Supply		500mA		Vcc=5V, depend on FPGA circuit.
Board Size		75x35mm		
Block type		20 items		
Clock type	1.953kHz		128MHz	17 types, 128, 64, 32, 16･･･MHz
CIC gain	0dB		60dB	Depend on Decimation rate.
Decimation rate	1		32000	
AWG data size		4095		12bit x 4095 word x 2ch
Interface to PC		USB 2.0		FT232HL 12Mbps