Recombination SDR signal processing blocks





User Manual



http://radiun.net/

© Radiun 2018 JAPAN Model:SBH-1 Revision A

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Features

The SDR Block HF is LF to HF band Transceiver based on the SDR technology. SDR is consisted of 20 or more items of signal processing blocks on the FPGA. Connections of these SDR blocks are recombined by software control without FPGA compile and configuration.

To recombine SDR blocks and capture wave data to PC, The SDR Block HF are providing easy access to user USB connection.

By using SDR Block HF own EXCEL macro SDR_ASM, SDR blocks are recombined and capture wave data easily via USB. A documented USB bridge FT232HL SPI allows developers to create new applications.

The SDR Block HF provides SDR experiment features ideally suited to industrial, scientific and educational applications.

High resolution NCC

Generate 5Hz to 32MHz 5Hz step Sin wave. Adjustable Amp, Phase and DC offset independently.

Variable Decimation filter

4 steps CIC filter is adjustable decimation rate 1 to 32000.

4096 word AWG x2ch

12bit x 4096 x 2ch AWG Clock adjustable 128MHz to 2kHz.

JTAG DIP 2x5 pins

Rewriteable CONFIG data accompanied with updating FPGA revision.

18x17 Matrix BUS Switch

Large 18 x 17 size matrix connection of SDR blocks is build from 17 rows and 18 columns of 12bit parallel BUS.

17 select CLK freq.

Each SDR blocks are able to select 17 steps of Clock frequency independently.

40dB LNA x2ch for R>

LNA is TI OP amp LMH6626. GBW 1.5GHz, $1nV/\sqrt{Hz}$. Gain 40dB and 20dB buffer amp.

High speed USB

Up to 12Mbps available allows developer create real time signal processing applications on the PC.

Key Features

RX/TX Frequency Range: 10kHz~32MHz RX/TX Bandwidth: 32MHz(64Msps)/ch ADC: 10bit 64Msps x2ch for RX input ADC: 12bit 1Msps for Audio input DAC: 10bit 64Msps for TX output PWM: 11bit 64ksps for Audio output Sensitivity: -110dBm/10kHz typ. S/N=10dB TX output: 1Vp-p diff (No Load) NCO: 64Msps 5Hz resolution x2ch Digital filter: CIC x2ch Variable Decimation AGC: Variable 17 speed response AWG: 12bit x 4096 x 2ch Wave Capture: 12bit x 1024 x 2ch via USB Other blocks: Adder, Mixer, Square, Square Root and Constant level. USB: FTDI FT232HL SPI in MPSSE mode Power: DC 5V 500mA via USB available Size: 3.0 x 1.4 inch 2 x 28 pin DIP

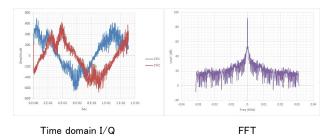
Applications

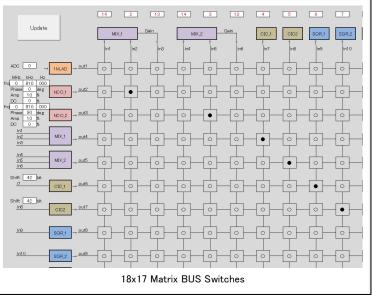
Amateur Radio Transceiver, Spectrum Analyzer, VNA, AWG, Signal Generator, Ultra Sonic Rader, Logger



Controller of the SDR Block HF

of SDR blocks, change parameters and clocks, AWG data transfer and capturing wave data.





Quick Start

1. Install FTDI Driver (Windows10)

Currently Supported D2XX Drivers:

https://www.ftdichip.com/Drivers/D2XX.ftml

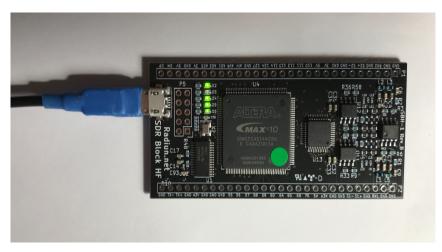
| FTDI Chip | Future Technology Devices International Ltd. THE USB BRIDGING SOLUTIONS SPECIALISTS |
|--|--|
| <u>Home</u> | D2XX Direct Drivers |
| <u>Products</u> <u>Drivers</u> | This page contains the D2XX drivers currently available for FTDI devices. |
| VCP Drivers | For Virtual COM Port (VCP) drivers, please click here. |
| D2XX Drivers D3XX Drivers | Installation guides are available from the Installation Guides page of the Documents section of this site for selected operating systems. |
| <u>Firmware</u> | |
| Support | D2XX Drivers |
| <u>Android</u> <u>EVE</u> <u>MCU</u> <u>Sales Network</u> | D2XX drivers allow direct access to the USB device through a DLL. Application software can access the USB device through a series of DL function calls. The functions available are listed in the D2XX Programmer's Guide document which is available from the Documents section of this site. |
| <u>Web Shop</u> <u>Newsletter</u> | Programming examples using the D2XX drivers and DLL can be found in the Projects section of this site. |

| | | | | Proce | ssor Architec | ture | |
|---------------------|-----------------|------------------|------------------|--|--|------|--|
| Operating System | Release Date | x86 (32- bit) | x64 (64- bit) | ARM | MIPS | SH4 | Comments |
| Windows* | 2017-08-30 | 2.12.28 | 2.12.28 | Clie | ck | - | WHQL Certified. Includes VCP and D2XX. Available as a setup executable Please read the Release Notes and Installation Guides. |
| Windows RT | 2014-07-04 | 1.0.2 | - | 1.0.2 | | - | A guide to support the driver (AN_271) is available here |
| Linux | 2018-06-22 | 1.4.8 | 1.4.8 | 1.4.8 ARMv5 soft-float 1.4.8 ARMv5 soft-float uClibc 1.4.8 ARMv6 hard- float (sults Raspberry PI) 1.4.8 ARMv7 hard- float | 1.4.8 MIPS32 soft-float 1.4.8 MIPS32 hard-float 1.4.8 MIPS openwrt- | | If unsure which ARM version to use, compare the output of readelf and file commands on a system binary with the content of release/build/libfd2xx.txt in each package. ReadMe Video Install Guide |

| Ⅰ · · · · · · · · · · · · · · · · · · · | | Click | _ | □ × + |
|---|---|--|--------------|--|
| JIG2 | VD-ROM(実践編) Inios2e_blk | ↓ マ すべて 展開 | | |
| ドキュメント OneDrive ドキュメント | 展開先 Static G ftd2xx.h ftdibus | すべて展開 このフォルダー内のすべての項目を 展開します。 | 8 KB 7 KB | in the second se |
| age 画像 1 添付ファイル S PC | √ ftdibus i ftdiport √ ftdiport | セットアップ情報 セキュリティ カタログ セットアップ情報 | | |
| ▶ 3D オブジェクト ▶ ダウンロード ▶ デスクトップ | | | | |
| 📔 ドキュメント խ ピクチャ 😰 ビデオ | | | | |
|) ミュージック し OS (C:) し DATA (D:) | | | | |
| ◎ DVD RW ドライブ (E:) D\ ▲ ネットワーク 8 個の項目 ↓ 状況: 24 共有 ↓ | v < | | | |

Unzip and locate download file to Desktop or any folder.

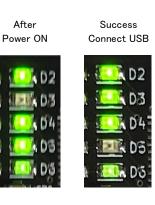
2. Connect PC and SBH-1 board via USB



Connect USB cable to PC. Check LED light on like picture above.



Launch an Excel sheet "SDR ASM" and open Worksheet "Blocks". Then click "Update" button to send any data to SBH-1 board.

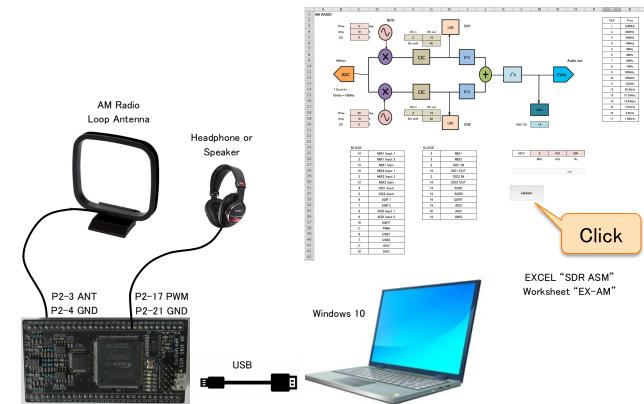


Check LED after click "Update" button. D2 : Divided master clock 1sec interval D3 : NCO Reset. 0:Reset 1:Run D4 : SPI CE 0:Enable 1:Disable D5 : SPI CLK 0:No Clock 1:Clocking D6 : FTDI 12MHz CLK

3. Execute Diagnostic (DIAG)

| | | | - | | _ | | - | | | ck | | | - | | | | | |
|----------|----------|-------------|--------------|------|--------|--------------|-------------|--|---------------------|---------|-----------------|-----------------|-------------|----|---------------|------------|---------------|--------|
| | A | В | C | D | E | F | G | H I | , OII | CK | M | N | 0 | Р | Q | R | S | Т |
| 1 2 | DIAG | To check 64 | Asps decice. | | | Do not conne | ct any PIN. | | | | | | | | | | | |
| 3 | Max | 1023 | 1023 | 378 | 335 | 72 | 68 | | | | | | | | | | | |
| 4 | Min | -1024 | -1024 | -468 | -367 | -92 | -40 | DIAG | | | | | | | | | | |
| 5 | | | | | | | | DIAG | | | | | | | | | | |
| 6 | Judge | PASS | PASS | PASS | PASS | PASS | PASS | | NCO Output | | | MIX Outp | ut | | | ADC | Output | |
| / | | | | | | | | | | | | | | | | | | |
| 8 | | NCO | Output | MIX | Output | ADC 0 | Dutput | 1500 | | | 1000 | | | | 500 | | | |
| 9 | | CH1 | CH2 | CH1 | CH2 | CH1 | CH2 | | | | 800 | | | | 500 | | | |
| 10 | 0 | 1023 | 908 | -4 | 40 | 4 | 36 | 1000 | | | 600 | | | | | | | |
| 11 | 1 | 198 | -1005 | 118 | 17 | 0 | 4 | | | | 400 | | | | 250 | | | |
| 12 | 2 | -490 | -903 | 136 | -85 | -12 | 20 | 500 | | | 200 | Mary | | | | | | |
| 13 | 3 | -952 | -375 | -19 | 56 | -20 | 8 | 0 | | | 0 | | É | | | | | |
| 14 | 4 | -971 | 326 | -8 | -19 | 0 | 44 | 0 | | | -200 | 4.5 | | | 0 | | 1 | |
| 15 | 5 | -542 | 871 | -124 | -67 | -32 | 20 | -500 | | | | 100 | | | | | | |
| 16 | 6 | 147 | 1013 | 19 | -4 | -8 | 16 | | | | -400 | | | | -250 | | | |
| 17 | 7 | 766 | 678 | -87 | 109 | -56 | 16 | -1000 | | | -600 | | | | -230 | | | |
| 18 | 8 | 1023 | 37 | 4 | 140 | 12 | 20 | | | | -800 | | | | | | | |
| 19 | 9 | 807 | -630 | 65 | 75 | -44 | 20 | -1500 | | | -1000 | | | | -500 | | | |
| 20 | 10 | 214 | -1001 | 19 | 3 | 36 | 12 | -1500 | -500 500 | 1500 | -1000 | -500 0 | 500 10 | 00 | -500 | -250 | 0 250 | 500 |
| 21 22 | 11 | -480 | -905 | 102 | -62 | -32 | 12 | | | | | | | | | | | |
| 22 | 12 | -951 | -386 | 13 | -38 | -8 | 20 | | | | | | | | | | | |
| 23 | 13 | -975 | 314 | -37 | -94 | -12 | 12 | | PASS Sample | | | PASS Sam | ple | | | PAS | S Sample | |
| 25 | 14 | -546 | 864 | -105 | -59 | -24 | 12 | 1500 | | | 1000 | | | | 500 | | | |
| 25 | 15 | 139 | 1014 | -138 | 26 | -32 | 32 | 1300 | | | 1000 | | | | 500 | | | |
| 27 | 16 | 753 | 693 | 12 | -16 | -32 | 48 | 1000 | | | _ | | | | | | | |
| 28 | 17 | 1022 | 41 | 0 | 40 | -8 | 28 | | | | 500 | _ | | | 250 | | | |
| 29 | 18 | 810 | -627 | -14 | -16 | -4 | -4 | 500 | | | _ | 2400 | | | - | | | |
| 30 | 19 | 226 | -1000 | 98 | 16 | 28 | -8 | 0 | | | 0 | | - | | - | | | |
| 31 | 20 | -469 | -909 | 0 | 0 | -20 | 4 | 0 | | | 0 | 1.00 | | | 0 | | | |
| 32 | 21 | | -401 | 59 | -170 | -24 | | -500 | | | _ | | | | | | T | |
| 53 | 22 23 | -979 | 303 863 | -43 | -113 | -64 | 28 | | | | -500 | | | | -250 | | | |
| 34 | 23 | -555 | 1015 | -87 | -50 | -24 | 32 | -1000 | | | | | | | | | | |
| 55 | 24 | 750 | 696 | -1// | 32 | -16 | 20 | -1500 | | | -1000 | | | | + | | | |
| 36 | 25 | 1022 | 53 | 0 | -62 | 24 | 28 | -150 | 0 -500 500 | 1500 | | 500 0 | 500 10 | | -500 | | | |
| 37 | 20 | 817 | -617 | 12 | 15 | -20 | 8 | -150 | 0 -500 500 | 1200 | -1000 | -500 0 | 500 10 | | -500 | -250 | 0 250 | 500 |
| 38 | 27 | 229 | -997 | 256 | 45 | -20 | 4 | Normal Street St | | | - | | | | | | | |
| 39 | 29 | -462 | -997 | -70 | 40 | -28 | -20 | Testing NCO | Phase , Amp, DC off | eat and | Testing Mixer G | ain Amn and C | look timing | | Testing LNA (| ain Noise | DC offeet and | Clock |
| 10 | 30 | -940 | -404 | -70 | -19 | -28 | 20 | Clock timing | | out and | error. | an, song arid o | ous utting | | timing error. | am, Hoise, | Do onset and | oloun. |
| | | -340 | -404 | 0 | -19 | -28 | 20 | GIOCK TIMING | arror. | | error. | | | | uning error. | | | |

Disconnect all of the SBH-1 pins except USB. Launch an Excel sheet "SDR ASM" and open Worksheet "DIAG". Then click "DIAG" button to diagnose the SBH-1 board itself automatically.

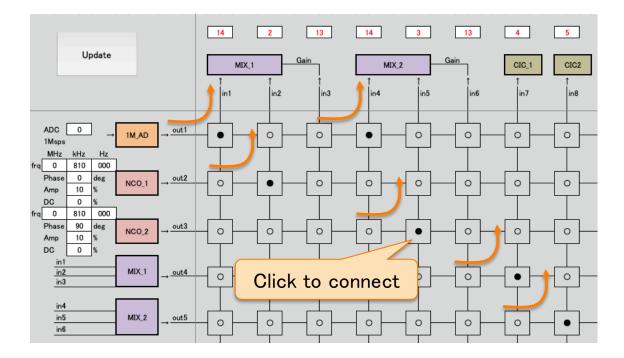


4. Build AM RADIO

Connect Loop antenna and headphone to SBH-1. Launch an Excel sheet "SDR ASM" and open Worksheet "EX_AM". Click "Update" button to build AM RADIO circuit on the FPGA.

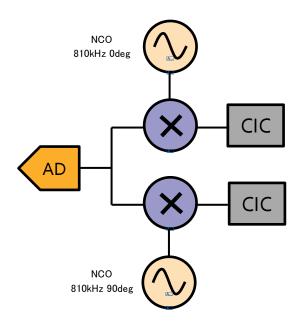
Define Blocks

1. Define Block Diagram



A FPGA on the SBH-1 consists of 20 items of signal processing brocks and 18x16 matrix BUS switch. BUS switch is software controlled via USB like above. Click to connect BUS on the cross point on Worksheet "Blocks".

The above example is shown as follows.



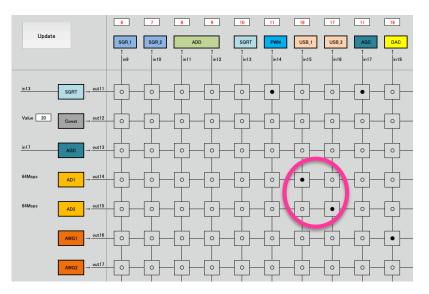
2. Define Clock Frequency

| | 2 | 2 | 2 | 14 | 2 | 14 | 14 | 14 | 14 | 14 | 14 | 2 |
|----------------------|---------|---------|-------|-------|-------|-------|-------|-------|---------|-------|-------|------|
| Update | MIX_1 | MIX_2 | CIC | .1 | CIC | 2 | SQR_1 | SQR_2 | SQRT | ADD | AGC | AWG |
| | î İn | t in | н | LO | н | LO | in | în. | t in | in | in | in |
| CLK1 128MHz → out | -0- | -0 | -[0] | -0- | -0- | -[0] | -[0] | -[0] | -[0] | -[0] | -0- | -0- |
| CLK2 64MHz → out | -• | | | -[-]- | -• | -[-]- | -[0] | -[-] | -[-] | -[0] | -[-]- | -• |
| CLK3 32MHz → out | -[0]- | -[0]- | -[0]- | -[0]- | -[0] | -[0] | -[0] | -[0] | -[0] | -[0]- | -[0]- | |
| CLK4 16MHz → out | -[0] | -0- | -[-]- | -[0]- | -[0] | -[-]- | -[0] | -[0] | -[-] | -[0] | -[-] | -0- |
| CLK5 8MHz → out | -[0] | -[0] | -[| -[0]- | -[-] | -[-]- | -[-] | -[-] | -[-] | -[0] | -[-]- | -[0] |
| CLK6 4MHz → out | -[0]- | -[0] | -[0] | -0- | -[0]- | -[0] | -[0] | -[0] | -[0] | -[0] | -[0] | -0- |
| CLK7 2MHz → out | -[0] | -[0] | -[0]- | -0- | -[0] | -[0]- | -[0] | -[0] | -[0] | -[0] | -0- | -0- |
| CLK8 1MHz → out | -[0]- | -[0]- | -[-]- | -[0]- | -[0]- | -[-]- | -[0] | -[-] | -[-] | -[0] | -[-]- | -[0] |

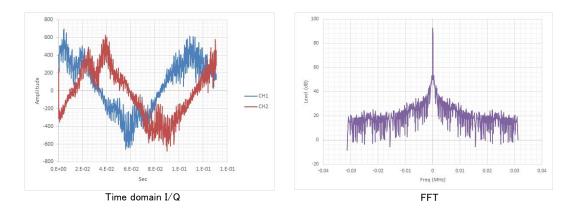
SDR signal processing blocks are able to select 17 frequency clocks. 2kHz to 128MHz. ADC and NCO are fixed 64MHz. It becomes possible to change CIC filter cutoff, adjustable AGC response and adjustable AWG speed.

Recommend Clock frequency is 64MHz or lower. Be careful, as the operation is not guaranteed 128MHz clocks.

3. Define Test points

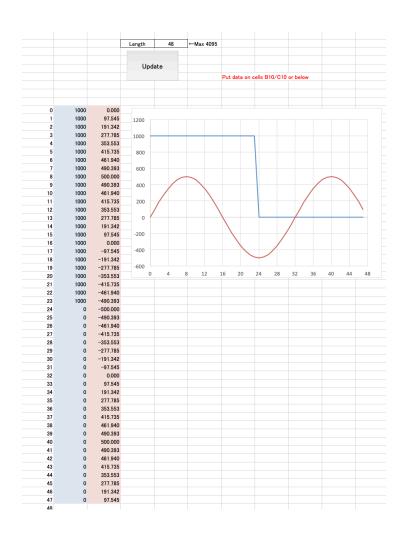


Test points (USB 1/2) can be placed in the circuit where you want to place. Results are displayed time domain like a Oscilloscope or frequency domain like a Spectrum analyzer on the EXCEL sheet.



AWG Arbitrary Waveform Generator

AWG1 and AWG2 blocks are the arbitrary waveform generator (AWG). Waveform editing and update wave data to RAM can be done with Excel ""SDR ASM" worksheet "AWG". AWG clock is selectable 2kHz to 64MHz.



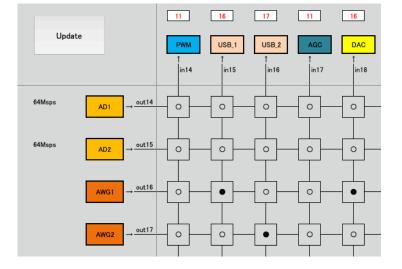
This is worksheet "AWG".

Available data is signed 12bit -2047 to 2047.

Data length up to 4095 words each.

Push "Update" to update wave data to RAM.

AWG continue generate wave repeat with the specified Data length.

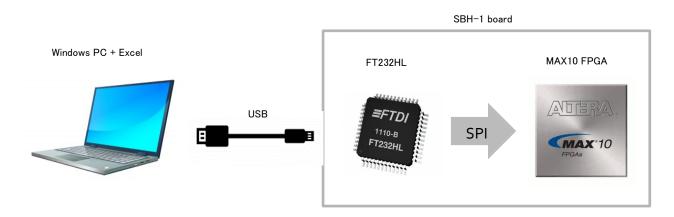


This is worksheet "Blocks".

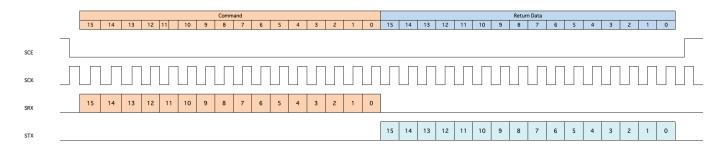
Here is an example for using the AWG1 and AWG2.

Waveform data of the AWG is output to the USB1, USB2 and DAC also.

SPI command



1. SPI Timing Chart



2. SPI Command List

| | | | | | | | Con | ıma | nd | | | | | | | | | | Return Data | |
|----|------------------|----|----|-----|----|--------|--------|-----|--------|------|------|------|------|------|-----|---|------------|---|---------------------------|--------------------|
| | | 15 | 14 | 13 | 12 | 11 10 | 9 | 8 | 7 6 | 5 | 5 4 | 4 | 3 | 2 | 1 | 0 | 15 14 13 1 | 2 | 11 10 9 8 7 6 5 4 3 2 1 0 | |
| | | | Fu | inc | | | | | Para | me | ter | | | | | | | | 16bit data | |
| | | | | | | | | | | | | | | | | | | | | |
| 0 | Capture Reset | 0 | 0 | 0 | 0 | Mode | • | | ADC | 5bit | t | | R | AM | CLK | (| | | Not use | Select ADC, Selec |
| 1 | Read RAM | 0 | 0 | 0 | 1 | СН | | R | AM A | ddr | ess | 11 | bit | | | | Write ADRS | 5 | Return RAM Data 12bit | Select RAM CH, R |
| 2 | NCO frequency | 0 | 0 | 1 | 0 | CH Ran | ige 3ł | bit | | | Fre | eq 8 | 8bit | : | | | | | Not use | Select NCO CH, S |
| 3 | Constant value | 0 | 0 | 1 | 1 | | | Co | nst v | alue | e 12 | bit | | | | | | | Not use | Set Constant value |
| 4 | Blocks define | 0 | 1 | 0 | 0 | | | XS | 5bit | | | | Y | 5bi | t | | | | Not use | Define Blocks (X |
| 5 | Clock define | 0 | 1 | 0 | 1 | | | XS | 5bit | | | | Y | 5bi | t | | | | Not use | Define Clock(X:I |
| 6 | NCO Phase | 0 | 1 | 1 | 0 | СН | | S | igned | l Ph | ase | 11 | bit | | | | | | Not use | Set NCO Phase |
| 7 | NCO Amp/DC | 0 | 1 | 1 | 1 | CH DC | | 5 | Signe | d A | mp/ | ′DC | :10 | bit | | | | | Not use | Set NCO Amplitud |
| 8 | CIC Bit shift | 1 | 0 | 0 | 0 | C | CIC1 6 | bit | | | | CI | IC2 | 6bit | t | | | | Not use | Specify the BIT po |
| 9 | AWG1 data update | 1 | 0 | 0 | 1 | | A | WG1 | 1 writ | e d | ata | 12 | bit | | | | Read ADRS | ; | Not use | Write AWG1 data t |
| 10 | AWG2 data update | 1 | 0 | 1 | 0 | | A | WG2 | 2 writ | e d | ata | 12 | bit | | | | Read ADRS | ; | Not use | Write AWG2 data t |
| 11 | AWG Size | 1 | 0 | 1 | 1 | | , | AWG | 6 Data | a Si | ze 1 | 2b | it | | | | | | Not use | Set AWG data leng |
| | | | | | | | | _ | | | _ | _ | | | _ | _ | | | | |

Select ADC, Select Capture Clock, Reset RAM address Select RAM CH, Read RAM data in FPGA to PC Select NCO CH, Set Frequency Set Constant value signed 12bit -2047~2047 Jefine Blocks (X :Input BUS line, Y:Output Bus line) Define Clock (X :Input BUS line, Y:Output Bus line) Set NCO Phase 0~804 (0~180deg) Set NCO Amplitude or DC offset 0~1023 (0~100%) Specify the BIT position to extract the signal Write AWG1 data to RAM in the FPGA with increment address. Set AWG data length and Reset RAM address.

3. Detail of the SPI Command

0. Capture Reset

| | | | | | | | Со | omm | and | | | | | | | | | | | | | | Re | turr | n Da | ta | | | | | | |
|---------------------------------------|----------------|--|--|--|--|--|----|-----|-----|--|---|---|----|----|----|----|----|----|-----|-----|------|-----|----|------|------|----|---|---|--|--|--|--|
| 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | | | | | | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | |
| | Func Parameter | | | | | | | | | | | | | | | | | | | 1 | 6bit | dat | ta | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 0 0 0 Mode ADC 5bit RAM CLK | | | | | | | | | | | (| | | | | | | | Not | use | | | | | | | | | | | | |

Before capturing the waveform in FPGA to RAM, execute this command and Reset both address to CH1 and CH2. At the same time, set the following parameters related to waveform capture.

| | Mo | de (Capture mode) | | | | | | | | | | | | |
|----------|----|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|
| | 0 | Single | | | | | | | | | | | | |
| 1 Stream | | | | | | | | | | | | | | |
| 0 | | PWM OFF | | | | | | | | | | | | |
| 1 | | PWM ON | | | | | | | | | | | | |

| ADC (1Msps ADC) 0 0 0 0 Analog IN 0 0 0 0 1 ADC1 0 0 0 1 0 0 0 0 0 0 1 0 0 0 | | | | | | | | | | | | |
|--|---|---|---|---|-----------|--|--|--|--|--|--|--|
| 0 | 0 | 0 | 0 | 0 | Analog IN | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | ADC1 | | | | | | | |
| 0 | 0 | 0 | 1 | 0 | ADC2 | | | | | | | |
| 0 | 0 | 0 | 1 | 1 | ADC3 | | | | | | | |

Stop capturing 2048 words in RAM Continually capture waveform repeatedly in RAM PWM output serves as a noise source, the PWM signal is stopped. Release PWM stop.

Select the input pin of the MAX10 ADC to Analog IN(AIN). Select the input pin of the MAX10 ADC to Analog IN(AD1). Select the input pin of the MAX10 ADC to Analog IN(AD2). Select the input pin of the MAX10 ADC to Analog IN(AD3).

| | | | R | AM CLK |
|---|---|---|---|---------------|
| 0 | 0 | 0 | 0 | Not Available |
| 0 | 0 | 0 | 1 | 128MHz |
| 0 | 0 | 1 | 0 | 64MHz |
| 0 | 0 | 1 | 1 | 32MHz |
| 0 | 1 | 0 | 0 | 16MHz |
| 0 | 1 | 1 | 1 | 8MHz |
| 0 | 1 | 1 | 0 | 4MHz |
| 0 | 1 | 0 | 1 | 2MHz |
| 1 | 0 | 0 | 0 | 1MHz |
| 1 | 0 | 1 | 1 | 500kHz |
| 1 | 0 | 1 | 0 | 250kHz |
| 1 | 0 | 0 | 1 | 125kHz |
| 1 | 0 | 0 | 0 | 62.5kHz |
| 1 | 1 | 1 | 1 | 31.25kHz |
| 1 | 1 | 1 | 0 | 15.63kHz |
| 1 | 1 | 0 | 1 | 7.81kHz |
| 1 | 1 | 1 | 0 | 3.9kHz |
| 1 | 0 | 1 | 1 | 1.95kHz |

Set the clock for loading the waveform into the RAM in FPGA.

1. Read RAM

| | | | | | | Cor | mma | and | | | | | | | | | | | | | | Re | eturi | ו Da | ta | | | | | | |
|----|---------------------------------------|--|--|--|--|-----|-----|-----|--|--|--|--|--|---|----|------|-----|----|----|----|---|------|-------|------|-------|-------|------|---|---|---|--|
| 15 | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | | | | | | | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | Func Parameter | | | | | | | | | | | | | | | | | | | | 1 | 6bit | dat | ta | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 0 0 1 CH RAM Address 11bit | | | | | | | | | | | | | | W | rite | ADF | ۲S | | | | Ret | urn I | RAM | I Dat | ta 11 | 2bit | | | | |

Specify the CH and address of the RAM to be read and obtain its contents as Return.

| | СН |
|---|-----|
| 0 | CH1 |
| 1 | CH2 |

Select CH of RAM to be read.

| | | | RAM | Add | ress | 5 1 1 | bit | | | | | | | | |
|---|---|---|-----|-----|------|-------|-----|---|---|---|--|--|--|--|--|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | |
| | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | | | |

Return the RAM contents of the address specified here as Return Data. Address=0

Address=1

Address=2046 Address=2047

Return the upper 4 bits of the address currently written to the RAM. This is for Stream captureing mode.

| N | /rite | ADR | S |
|---|-------|-----|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |

Writing RAM address 128 or upper.

Writing RAM address 256 or upper.

Writing RAM address 512 or upper.

Writing RAM address 1024 or upper.

| | | | Retu | rn R | AM [| Data | 12 | bit | | | |
|---|---|---|------|------|------|------|----|-----|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

It returns the data of the specified RAM address in 2's complement.

Data=2047 Data=1 Data0 Data=-1

Data=-2047

2. NCO Frequency

| | Command 5 14 13 12 11 10 9 8 7 6 5 4 3 2 1 | | | | | | | | | | | | | | | | | | | | | Re | eturi | ו Da | ta | | | | | | | | |
|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|----|----|----|----|------|----|------|-------|------|----|---|---|---|---|---|---|--|--|
| 15 | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 | | | | | | | | | | | | | | 0 | 15 | 14 | 13 | 12 | 2 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| | Func Parameter | | | | | | | | | | | | | | | | | | | | 1 | 6bit | dat | a | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Set the freq data of 24 bits by dividing it into 8 bit by 3 times.

F1= Round(Fo and 0xFF)

F2= Round(Fo and 0xFF00) / 0x100

F3= Round(Fo and 0xFF0000) / 0x10000 After set NCO, this reset is always executed to synchronize the phase CH1 and CH2.

Not use

Fo = Round(F * 0.205887) F(Hz)

Set the NCO frequency.

0 0 1 0 CH Range 3bit

| | СН |
|---|-----|
| 0 | CH1 |
| 1 | CH2 |

Set channel of the NCO .

Lower 8 bit data

Middle 8 bit data

Upper 8 bit data

Release of NCO reset.

Freq 8bit

| | | Ra | inge (Freq range) |
|---|---|----|-------------------|
| 0 | 0 | 0 | LOW |
| 0 | 0 | 1 | MID |
| 0 | 1 | 0 | Н |
| 1 | 1 | 0 | NCO Reset ON |
| 1 | 1 | 1 | NCO Reset OFF |

| | | F | req | 8bit | | | |
|---|---|---|-----|------|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Frequncy data F1, F2 or F3

| 1 | |
|-----|--|
| 2 | |
| | |
| 254 | |
| 255 | |

3. Constant Value

| | | | | | | | Сс | omm | nand | | | | | | | | | | | | | | Re | turr | ו Da | ta | | | | | | |
|----|--|----|----|----|----|----|----|-----|------|------|-------|-------|---|---|---|---|----|----|----|----|----|------|-----|------|------|----|---|---|---|---|---|---|
| 15 | 5 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Func Parameter | | | | | | | | | | | | | | | | | | | | 1 | 6bit | dat | ta | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | | 0 | 1 | 1 | | | | С | òns | t va | lue 1 | l 2bi | t | | | | | | | | | | | Not | use | | | | | | | |

Set the constant value. Sometimes it is taken as DC offset.

| | | | Co | onst | valu | le 1 | 2bit | | | | |
|---|---|---|----|------|------|------|------|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Data=2047 Data=1 Data0 Data=-1 Data=-2047

4. Blocks Define, 5. Clock Define

| | | | | | | | Со | mm | and | | | | | | | | | | | | | | Re | eturr | ו Da | ta | | | | | | |
|----|-------------------------------------|--|--|--|--|--|----|----|-----|--|--|--|--|---|----|----|----|----|----|----|---|------|-----|-------|------|----|---|---|---|---|--|--|
| 15 | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 | | | | | | | | | | | | | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| | Func Parameter | | | | | | | | | | | | | | | | | | | | 1 | 6bit | dat | a | | | | | | | | |

| 0 | 1 | 0 | 0 | X 5bit | Y 5bit | Not use |
|---|---|---|---|--------|--------|---------|
| 0 | 1 | 0 | 1 | X 5bit | Y 5bit | Not use |

Define Blocks or Define Clock.

| | > | (5bi | t | | | Y | ′ 5bi | t | | | |
|---|---|-------|---|---|---|---|-------|---|---|--------|--------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X = 0 | Y = 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | X = 1 | Y = 1 |
| | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | X = 30 | Y = 30 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X = 31 | Y = 31 |

6. NCO Phase, 7. NCO Amplitude or DC Offset

Signed Amp/DC 10bit

| | Command | | | | | | | | | | | | | | | Return Data | | | | | | | | | | | | | | | | |
|----|---------------------------------|---|----|----|----|----|---|---|---|---|---|---------|------------|---|---|-------------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 1 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | Func Parameter | | | | | | | | | | | | 16bit data | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 1 1 0 CH Unsigned Phase 11bit | | | | | | | | | | | Not use | | | | | | | | | | | | | | | | | | | | |

Set the NCO phase, amplitude and DC offset.

1 CH DC

0 1

1

| | СН |
|---|-----|
| 0 | CH1 |
| 1 | CH2 |

Set the NCO channel.

| | | | Sign | ed Pl | hase | e 11 | bit | | | | | | | | |
|---|---|---|------|-------|------|------|-----|---|---|---|--|--|--|--|--|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | |
| | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | | | |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | | | | | |

| Set th | e NCO phase |
|--------|-------------------|
| 0 | Phase = 0.0 deg |
| 1 | Phase = 0.2 deg |
| | |
| 803 | Phase = 179.8 deg |

804 Phase = 180.0 deg

Select Amplitude or DC offset

Ralation betoween freq and phase resolution.

Not use

| | Phase | MHZ |
|----|-------|-----|
| | 5.6 | 1 |
| | 28.1 | 5 |
| | 56.3 | 10 |
| ←l | 90.0 | 16 |
| ←l | 180.0 | 32 |

Limit of I/Q Limit of Generate

| | DC |
|---|-----------|
| 0 | Amplitude |
| 1 | DC offset |

| | | Sig | ned / | Amp. | /DC | 10 | oit | | Signed Amp/DC 10bit | | | | | | | | | | | | | |
|---|---|-----|-------|------|-----|----|-----|---|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | | |

Set the NCO Amplitude or DC offset.

| 0 |
|-------|
| -1 |
| -1023 |
| |

1023 1

14

8. CIC Bit Shift

| | Command | | | | | | | | | | | | | | | Return Data | | | | | | | | | | | | | | | | |
|----|---------|----|----|----|---------------------|----|---|---|---|------|------|---|---|---|---|-------------|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | ŀ | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | F | un | IC | | | | | | P | aran | nete | r | | | | | 16bit data | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | | 0 | 0 | CIC1 6bit CIC2 6bit | | | | | | | | | | | Not use | | | | | | | | | | | | | | | | |

Specify the position to extract 12 bits from the internal register of the CIC.

| 2kHz, the gain is maximum 60dB |
|--------------------------------|
| 2 |

9-10. AWG1/2 Data Update, 11 AWG Size

| | Command | | | | | | | | | | | | | | | | Re | eturi | n Da | ta | | | | | | |
|----|---------------------------------------|--|--|--|--|--|--|--|--|------------|----|----|----|----|----|----|----|-------|------|----|---|---|---|---|---|---|
| 15 | 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | | | | | | | | | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | Func Parameter | | | | | | | | | 16bit data | | | | | | | | | | | | | | | | |

| 1 | 0 | 0 | 1 | AWG1 write data 12bit | Read ADRS | Not use | | | | |
|---|---|---|---|-----------------------|-----------|---------|--|--|--|--|
| 1 | 0 | 1 | 0 | AWG2 write data 12bit | Read ADRS | Not use | | | | |
| 1 | 0 | 1 | 1 | AWG Data Size 12bit | Not use | | | | | |

Transfer AWG data to RAM in the FPGA.

| | AWG1/2 write data 12bit | | | | | | | | | | | | | | |
|---|-------------------------|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |

Data is written to RAM of AWG 1/2, and write address is counted up Data=2047

| Data-2047 |
|------------|
| Data=1 |
| Data0 |
| Data=-1 |
| Data=-2047 |
| |

| Read ADRS | | | | | | | | | | | |
|-----------|---------|---|---|--|--|--|--|--|--|--|--|
| 0 | 0 0 0 1 | | | | | | | | | | |
| 0 | 0 | 1 | 0 | | | | | | | | |
| 0 | 1 | 0 | 0 | | | | | | | | |
| 1 | 0 | 0 | 0 | | | | | | | | |

Returns the upper 4 bits of the address currently being read by the RAM. This is for Stream transmit mode.

Reading RAM address 128 or upper.

Reading RAM address 256 or upper.

Reading RAM address 512 or upper.

Reading RAM address 1024 or upper.

| | AWG Data Size 12bit | | | | | | | | | | | | | |
|---|---------------------|---|---|---|---|---|---|---|---|---|---|--|--|--|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | | |
| | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | |

Set the data length of AWG after writing data, write address is reset

| Size = 1 |
|-------------|
| Size = 2 |
| |
| Size = 4094 |

Size = 4095

Sample Program (VBA)

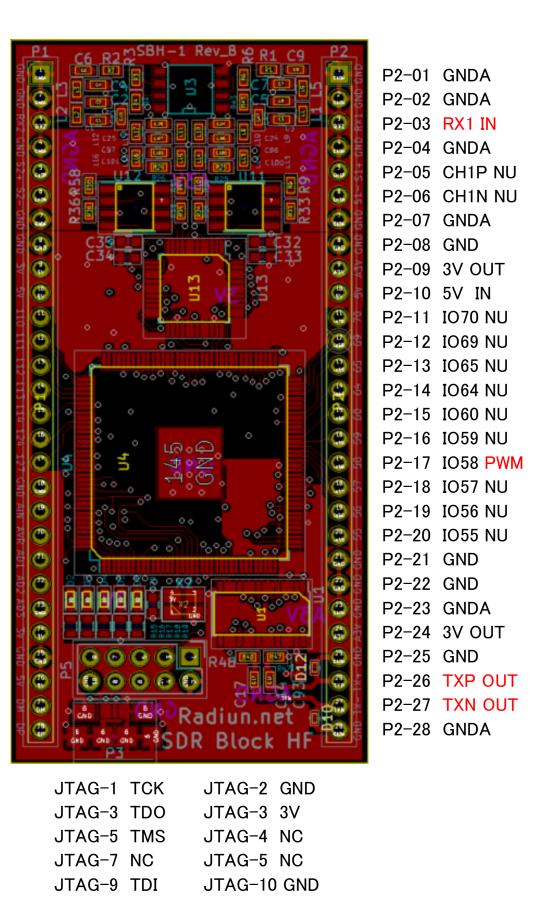
This sample program is to read the waveform from the RAM in the FPGA and list the numerical value on the EXCEL sheet when Button is pushed.

```
Sub Oscillo_Click()
    Dim clk As Long
    ' Read Setting CLK and PWM ON/OFF
    clk = Cells(3, 5)
    pwmsw = Cells(12, 10)
    ' Open SPI BUS
    cmd = OpenSPI(0)
    ' RAM addres reset
                                                 ' Continue mode
    ret = rxSPI(512 + clk + 1024 * pwmsw, 0)
    ret = rxSPI(clk + 1024 * pwmsw, 0)
                                                 ' Single mdoe
    ' Start Capture
    ret = rxSPI(4096, 0)
    ' Read RAM CH1
    ch = 0
    For n = 0 To 1023
        ret = rxSPI(ch * 2048 + 4096 + n, 0)
                                                 ' ADC data
        dat = (ret And 4095)
        adrs = (ret And 61440)
                                                 ' RAM current address
        If dat > 2047 Then Cells(n + 10, 3) = dat - 4096
        If dat < 2047 Then Cells(n + 10, 3) = dat
    Next
    ' Read RAM CH2
    ch = 1
    ret = rxSPI(ch * 2048 + 4096 + n, 0)
    For n = 0 To 1023
        ret = rxSPI(ch * 2048 + 4096 + n, 0)
                                                 ' ADC data
        dat = (ret And 4095)
                                                 ' RAM current address
        adrs = (ret And 61440)
        If dat > 2047 Then Cells(n + 10, 4) = dat - 4096
        If dat < 2047 Then Cells(n + 10, 4) = dat
    Next
    ' PWM ON
    ret = rxSPI(0, 0)
    ' Close SPI BUS
    CloseSPI
```

End Sub

PIN Layout

P1-01 GNDA P1-02 GNDA P1-03 RX2 IN P1-04 GNDA P1-05 CH2P NU P1-06 CH2N NU P1-07 GNDA P1-08 GND P1-09 3V OUT P1-10 5V IN P1-11 IO110 NU P1-12 IO111 NU P1-13 IO112 NU P1-14 IO113 NU P1-15 IO114 NU P1-16 IO124 NU P1-17 IO127 NU P1-18 GNDA P1-19 ANAIN1 P1-20 VREF P1-21 ADCIN1 P1-22 ADCIN2 P1-23 GNDA P1-24 3V OUT P1-25 GND P1-26 5V IN P1-27 USB DM P1-28 USB DP

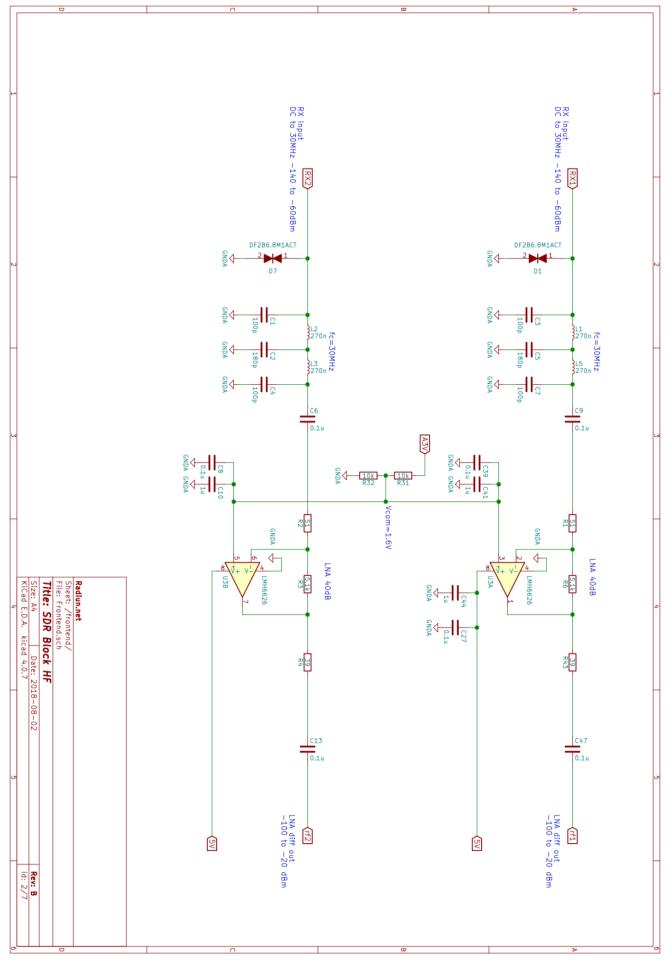


NU means Not Use pin but wired on the board. When you want to use it, you can use it by definition or added parts.

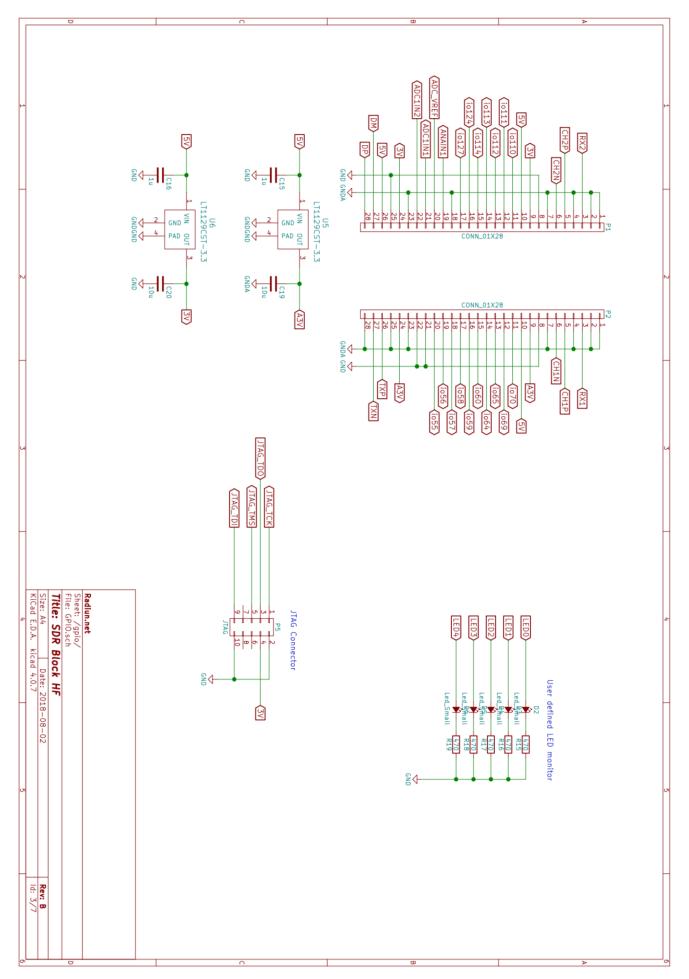
CH1P/N and CH2P/N are differential 64Msps ADC input to pass the 40dB LNA.

Schematics

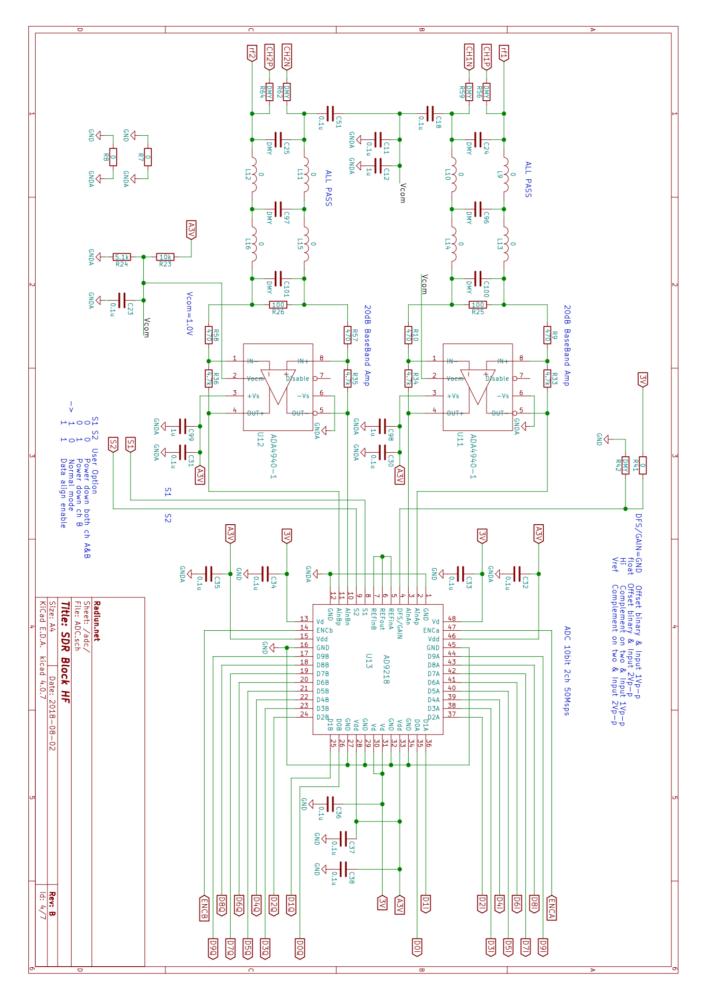




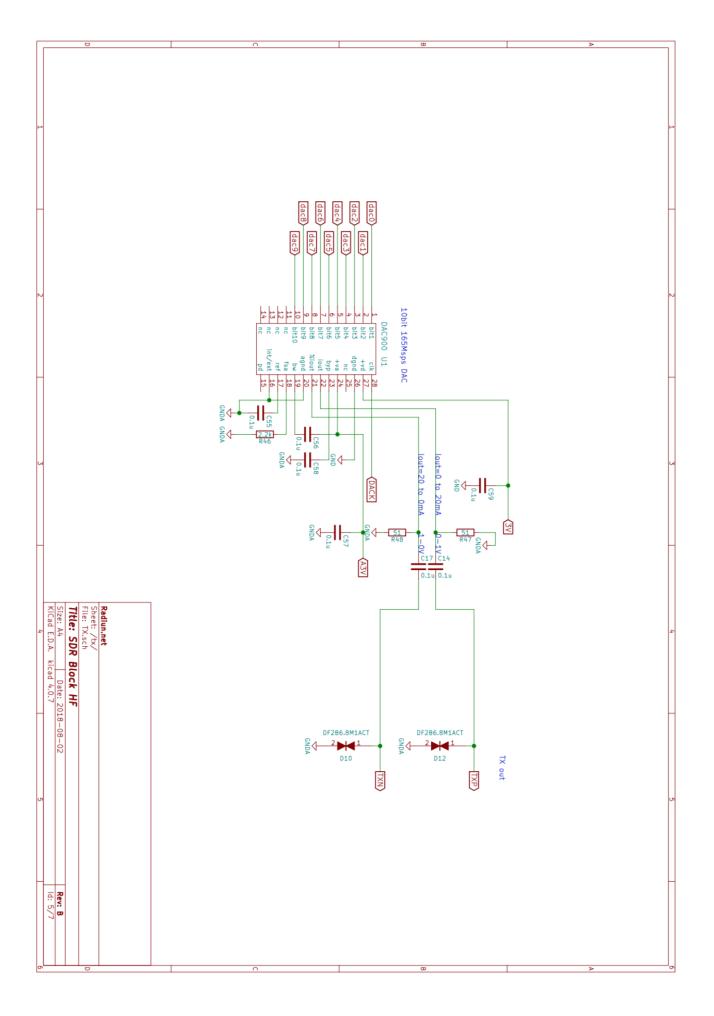
GPIO, JTAG, LDO, LED



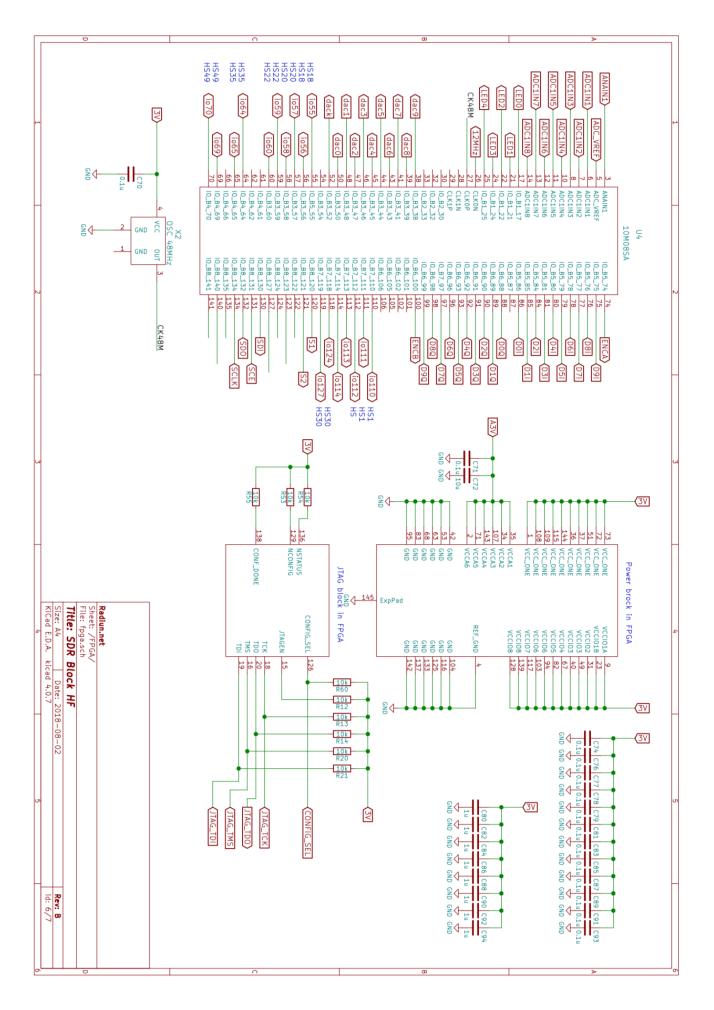
20dB Amp, 64Msps ADC



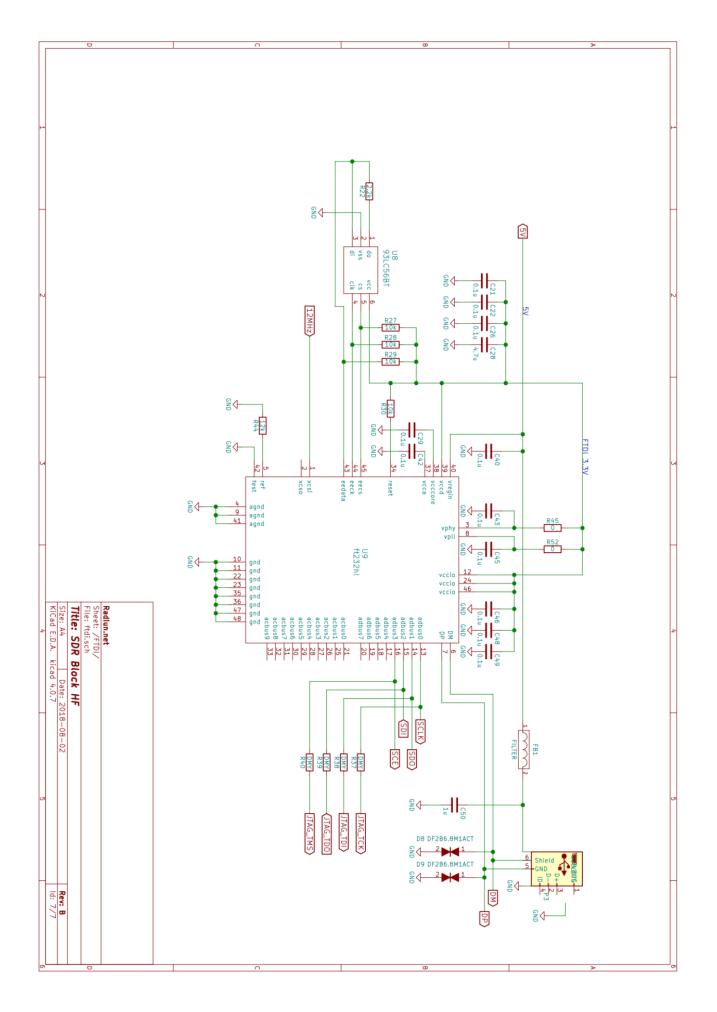
64Msps DAC, TX output



FPGA MAX10, TCXO



USB FTDI



Specifications

| | Min | Тур | Max | Remarks |
|-----------------|----------|--------------|--------|----------------------------------|
| Frequency Range | 10kHz | | 32MHz | Nyquist Limit = fsmp/2 |
| | 10kHz | | 16MHz | I/Q Limit = 90deg |
| Resolution | | 5Hz | | |
| RX ADC x2ch | | 10bit 64Msps | | AD9218-80Msps |
| AF ADC x1ch | | 12bit 1Msps | | MAX10 ADC |
| TX DAC x1ch | | 10bit 64Msps | | DAC900 165Msps |
| TX Output | | 1Vp-p | | Differential, No Load |
| RX Gain | | 60dB | | Total |
| | | 40dB | | LNA LMH6626 x2ch |
| | | 20dB | | Defferential OP amp ADA4940 x2ch |
| Noise Floor | | −160dBm/Hz | | RX input 1MHz |
| PWM Output | | 1Vp-p | | Differential, No Load |
| | | 11bit | | |
| | | 62.5ksps | | |
| Power Supply | | 500mA | | Vcc=5V, depend on FPGA circuit. |
| Board Size | | 75x35mm | | |
| Block type | | 20 items | | |
| Clock type | 1.953kHz | | 128MHz | 17 types, 128, 64, 32, 16…MHz |
| CIC gain | 0dB | | 60dB | Depend on Decimation rate. |
| Decimation rate | 1 | | 32000 | |
| AWG data size | | 4095 | | 12bit x 4095 word x 2ch |
| Interface to PC | | USB 2.0 | | FT232HL 12Mbps |

